

jc377 U.S. PTO
02/02/00

ASSISTANT COMMISSIONER FOR PATENTS

WASHINGTON, D.C. 20231

ATTENTION: BOX PATENT APPLICATION

Sir:

Transmitted herewith for filing is the patent application of

Inventor: **Sarit Neter**

For: **METHOD AND APPARATUS FOR COLOR INTERPOLATION**

Enclosed are:

- (X) 29 sheets of drawings.
- (X) Recordation form cover sheet with 1-page assignment.
- (X) A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- (X) A power of attorney form and copy of assignment.
- (X) Initial signed declaration by inventor.
- (X) Return prepaid postcard.

CLAIMS AS FILED

| FOR | NUMBER FILED | NUMBER EXTRA | RATE | FEE |
|--|-----------------|-----------------|-----------------------------|--------------|
| Basic Fee | | | \$345 | \$345 |
| Total Claims | 42 - 20 = | 22 × | \$9 | \$198 |
| Independent Claims | 4 - 3 = | 1 × | \$39 | \$39 |
| If application contains any multiple dependent claims(s), then add | | | \$130 | \$0 |
| | | | TOTAL FILING FEE | \$582 |

- (X) A check in the amount of \$582 to cover the filing fee is enclosed.
- (X) A check in the amount of \$40 to cover the assignment recording fee.
- (X) The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment to Account No. 11-1410. A duplicate copy of this sheet is enclosed.

jc511 U.S. PTO
09/496607
02/02/00

(X) Please use Customer No. 20,995 for the correspondence address.



Alex C. Chen
Registration No. P-45,591
Attorney of Record

H:\DOCS\ACC\ACC-1506.DOC:smn
020200

INTELLECTUAL PROPERTY LAW

KNOBBE, MARTENS, OLSON & BEAR

A LIMITED LIABILITY PARTNERSHIP INCLUDING
PROFESSIONAL CORPORATIONS

PATENT, TRADEMARK AND COPYRIGHT CAUSES

620 NEWPORT CENTER DRIVE

SIXTEENTH FLOOR

NEWPORT BEACH, CALIFORNIA 92660-8016

(949) 760-0404.

FAX (949) 760-9502

INTERNET WWW.KMOB.COM

JOHN W HOLCOMB
DAVID J MULLEN, III, PH.D
JOSEPH S. CIESFRANI
JOSEPH M. REISMAN, PH.D
WILLIAM R. ZIMMERMAN
GLEN L. TUTTALL
ERIC S. FURMAN, PH.D
DO TE KIM
TIRZAH ABE LOWE
GEOFFREY Y. IIDA
ALEXANDER S. FRANCO
SANJIVPAL S. GILL
SUSAN M. MOSS
JAMES W. HILL, M.D.
ROSE M. THIESSEN, PH.D
MICHAEL L. FULLER
MICHAEL A. GULIANA
MARK J. KERTZ
RABINDER N. NARULA
BRUCE S. ITCHKAWITZ, PH.D
PETER M. MIDGLEY
THOMAS S. MCCLENNAHAN
MICHAEL S. OKAMOTO
M. CHRISTINA THOMSON
JOHN M. GROVER
MALLARY K. MCCARTHY
LATEEF A. RAFAN
AMY C. CHRISTENSEN
SHARON S. NG
MARK J. GALLAGHER, PH.D
DAVID G. JANKOWSKI, PH.D
BRIAN C. HORNE
PAYTON J. LEMILLEUR

02/02/00

01 COUNSEL
JERRY L. SEELY

JAPANESE PATENT
KATSUNORI AOKI

EUROPEAN PATENT
MARTIN HILBERG

KOREAN PATENT
MINCHUL KIM

SCIENTISTS & ENGINEERS
(NON-LAWYERS)

RAIMOND J. SALENIENKS**
NEIL S. BARTFELD, PH.D.
DANIEL E. JOHNSON, PH.D.
JEFFERY KOEPEK, PH.D
KHURRAM RAHMAN, PH.D
JENNIFER A. HAYNES, PH.D
BRENDAN P. O'NEILL, PH.D
THOMAS Y. NAGATA
ALAN C. GORDON
PABLO S. HUERTA
LINDA H. LIU
MICHAEL J. HOLIHAN
YASHWANT VAISHNAV, PH.D.
MEGUMI TANAKA

* A PROFESSIONAL CORPORATION
† ALSO BARRISTER AT LAW (U.K.)
** U.S. PATENT AGENT

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Attorney Docket No. : YMEDIA.001A

Applicant(s) : Sarit Neter

For : METHOD AND APPARATUS FOR COLOR INTERPOLATION

Attorney : Alex C. Chen

"Express Mail"

Mailing Label No. : EL207479255US

Date of Deposit : February 2, 2000

I hereby certify that the accompanying

Transmittal in Duplicate; Specification in 36 pages; 29 sheets of drawings; **SIGNED** Declaration by Inventor in one pages; Recordation Form Cover Sheet and Assignment in two pages; Power of Attorney by Assignee in two pages; Small Entity Statement; Submission of Formal Drawings; Checks for Filing Fees; Return Prepaid Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and are addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Donald King

H:\DOCS\ACC\ACC-1510.DOC:smn\020200

201 CALIFORNIA STREET
SUITE 1150
SAN FRANCISCO, CALIFORNIA 94111
(415) 954-4114
FAX (415) 954-4111

501 WEST BROADWAY
SUITE 1400
SAN DIEGO, CALIFORNIA 92101-3505
(619) 235-8550
FAX (619) 235-0176

3801 UNIVERSITY AVENUE
SUITE 710
RIVERSIDE, CALIFORNIA 92501
(909) 781-9231
FAX (909) 781-4507

1875 CENTURY PARK EAST
SUITE 600
LOS ANGELES, CALIFORNIA 90067
(310) 407-5484
FAX (310) 407-5485

For: **METHOD AND APPARATUS FOR COLOR INTERPOLATION**

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL-ENTITY STATUS

I, the undersigned, do hereby declare that:

☒ I am an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: Y Media Corporation

ADDRESS OF CONCERN: 23172 Plaza Pointe Drive, Suite 285, Laguna Hills, CA 92653

I further declare that the above-identified small business concern qualifies as a small business concern as defined in 13 CFR 121.12, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both. I further declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention described in the patent or application identified above.

The individual, concern or organization identified above has not assigned, granted, conveyed or licensed, and is under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

If the rights held by the above-identified individual, concern or organization are not exclusive, each individual, concern or organization having rights in the invention are identified below. Each such individual, concern or organization must file separate verified statements averring to their status as small entities.

***NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27).**

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small-entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: Ian Olsen

TITLE OF PERSON (if not an owner or individual): President & CEO

ADDRESS OF PERSON SIGNING: 23172 Plaza Pointe Drive, Suite 285, Laguna Hills, CA 92653

SIGNATURE: 

H:\DOCS\ACCVACC-1459.DOC:smn
012100

DATE: 2.2.00

METHOD AND APPARATUS FOR COLOR INTERPOLATIONClaim of Priority

5 This patent application claims the benefit of U.S. Provisional Application No. 60/149,796 filed August 19, 1999, which is hereby incorporated herein by reference in its entirety.

Background of the InventionField of the Invention

10 The present invention relates to imaging systems, and in particular, to methods and systems for color interpolation.

Description of the Related Art

15 Conventional integrated circuit imaging devices include an array of light detecting elements or pixels which are interconnected to generate a signal representation of an image illuminating the device. Two common examples of conventional integrated circuit imaging devices are a charge coupled device (CCD) and a complementary metal oxide semiconductor (CMOS) image sensing device. Conventional imaging devices use one or more light detecting elements and charge storage elements. In order to produce a color image, the imaging devices separate the light into various color components by
20 filtering the light before the light strikes the light detecting elements. The array of light detecting elements is often deposited with a filter layer such that neighboring pixels may have different color filters and organized in a particular pattern.

25 Because each pixel is only capable of detecting a single color, conventional imaging devices require a process by which all of the color components are reconstructed for each pixel in order to maintain the original unfiltered array resolution. To reconstruct the color components, conventional imaging devices use a process of color interpolation that is performed after an analog signal associated with each pixel has been digitized. The conventional process of color interpolation performed after an analog signal associated with each pixel has been digitized requires conversion from
30 analog to digital (A/D) and may require extensive computations in order to achieve a high quality color presentation of the image. The A/D conversion and extensive

computations may require hardware, such as analog-to-digital (A/D) converters, memory, processors and software. The hardware and software may add to the complexity, size and expense of the imaging device and reduce the speed of the imaging process.

5 Conventional imaging devices also require color compensation for differences in the response of the various color filters and for variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. For example, when the primary color scheme is used, the response of an element that absorbs red light may be different than an element that absorbs blue light even when illuminated by
10 light of equal red and blue luminosity levels. When exposed to a flat light image having equal intensity and chromaticity levels throughout, typical CMOS or CCD arrays may generate analog signals having significant magnitude variations for the different color components. Accordingly, if the analog signals are used to reproduce the original image, the reproduced image colors will not match the original colors.

15 To overcome this problem, conventional imaging devices employ a process of color correction that is performed after the analog signals for each pixel have been digitized. One drawback of the conventional color correction process is a loss in color dynamic range that results from under-utilization of the A/D converter for some of the color components. Another drawback is increased computations that translates into
20 additional hardware, size, expense and/or reduced speed.

 The effect of loss in color dynamic range is particularly noticeable in the low light areas of an image that contains low as well as high light regions. The human eye is sensitive to minute changes in hue and saturation levels. A reduction in color component dynamic range may result in less vivid, plain, or flat images. Attempts to
25 correct this via hue or saturation enhancement filters may cause color distortion rather than color restoration.

 Another color compensation that integrated circuit color imaging devices require is for different illumination temperatures. The hue of a color component changes with respect to the ambient illumination. Thus, a white object under sunlight
30 conditions is perceived by the imaging device as white, but under fluorescent light conditions is perceived as light green.

To overcome this problem, conventional integrated circuit color imaging devices employ a process of white balance that is performed after the analog signals for each pixel have been digitized. Typically, each of the three processed color components, red, green or blue, is a convolution of the three colors. A drawback of the conventional white balance process is increased computations that translates into additional hardware and/or reduced speed.

The collection of signals read from the pixels represents the image viewed by the array. Each pixel represents a sample of the image and hence is a data value in the two-dimension image produced by the imaging system. Defect pixels, referred to as 'bad pixels,' do not contain a correct value and appear as artifacts. The bad pixels can reduce the image quality significantly. A bad pixel is caused by array defect and produces an output signal that significantly deviates from the mean output level of adjacent pixels when the exposure level of all pixels is substantially unified. Pixels that are significantly brighter than adjacent pixels in a unified dark frame are referred to as 'hot pixels,' while pixels that are significantly darker than adjacent pixels in a unified bright frame are referred to as 'dead pixels.'

The defect pixels are typically distributed in a random manner. However, a bad column (i.e. - a complete column is defective), or a blemish (i.e. - a cluster of neighboring pixels is defective) may occur and are typically discarded by the manufacturer. The manufacturer releases sensor arrays that contain random defect pixels in an amount that does not exceed a given limit, and the bad pixels are typically corrected. Both CCD and CMOS integrated circuit color imaging devices employ a process of bad pixel detection and correction. Conventionally, the detection step is performed off-line by the manufacturer. A bad pixel list is stored in the device. The correction step is typically performed after the analog signal for each pixel has been digitized.

Summary of the Invention

The present invention is directed to imaging methods and systems for flexibly addressing and processing imaging pixel sensor elements. The novel architecture of the present invention allows for a highly integrated, low cost imager with high speed

performance and good image quality. For example, the imaging system provides on-the-fly color interpolation, color compensation (also called color correction, color maximization or white balance) and/or fixed pattern noise reduction. The hardware and/or software related to on-the-fly color interpolation, color compensation and/or fixed pattern noise reduction may be provided on-chip.

One embodiment of an imaging system in accordance with the present invention comprises an array of pixel sensor cells arranged in rows and columns, a plurality of detection circuits, an array controller, a control circuit that allows for various programmable modes of pixel readout, and a programmable amplification stage that may be adjusted per pixel or per group of pixels. In accordance with one embodiment, the imaging system further includes a color filter layer deposited on the sensor array. The color filter may comprise, for example, Red, Green, and Blue filters organized in the Bayer pattern scheme. In one embodiment, the system further contains a circuit for performing one or more averaging operations.

One aspect of the present invention relates to an on-the-fly color interpolation apparatus and process that comprises a color reconstruction procedure performed during the sensor readout stage. The on-the-fly color interpolation process is capable of reading two or more consecutive rows and two or more consecutive columns simultaneously, summing some of the signals, and independently amplifying the signals with an optionally programmable gain amplifier. The on-the-fly color interpolation process is advantageously performed in an analog domain before an analog-to-digital conversion.

The on-the-fly color interpolation process of the present invention provides high speed of operation and reduced computational complexity with good color image quality. The on-the-fly color interpolation process is advantageously suited for many imaging applications today that do not require high color precision or high image quality, as well as those which do. For example, some high quality, digital cameras have modes of operation such as a 'preview' mode where image quality is less important than speed and implementation complexity.

One embodiment of the on-the-fly color interpolation process provides at least two modes of operation: a full resolution mode and a sub-sampling mode. Full

resolution mode is preferably used when high image quality is desired. In full resolution mode, each Red-Green-Blue (RGB) triplet needed for a color pixel representation is produced from a group of 2x2 pixels within the Bayer pattern. The four pixels are read out simultaneously, the two diagonally neighboring Green pixels are summed together, and the gain associated with the Green pixels is reduced in half. The resulting Green component is sent out with the diagonally neighboring Red and Blue pixels to produce one RGB triplet. Each subsequent RGB triplet shares one of the Green pixels and either the Red or Blue pixel of the preceding RGB triplet.

The sub-sampling mode may be used when a lower resolution image is desired, such as when a user previews an image. Sub-sampling is achieved via skipping pixels along the horizontal and/or the vertical axis of the pixel array. For a sub-sampling ratio of 1:j vertically and 1:k horizontally, where j, k are even, each RGB triplet that is needed for a color pixel representation is produced from a group of j by k pixels with the Bayer pattern. All Green pixels in the j*k neighborhood are averaged to produce the green component. Similarly, all of the Red pixels in the same neighborhood are averaged to produce the Red component, and all Blue pixels in the neighborhood are averaged to produce the Blue component. The three components are then sent out as the RGB triplet representing the j by k group of pixels. The sub-sampling process can be achieved by reading the j rows simultaneously.

Both the full resolution and the sub-sampling modes of operation can be further combined with a window readout mode where only a sub-region of the whole sensor array is read.

Another aspect of the present invention relates to an apparatus and process for color compensation or maximization. The color compensation process compensates for differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. The color compensation process of the present invention improves color dynamic range, decreases computations and hardware and improves speed of operation. The color compensation process of the present invention is advantageously performed in the analog domain before an analog-to-digital conversion. The color compensation process

of the present invention also improves white balance which is used to compensate colors for different illumination temperatures.

5 In one embodiment, the imaging system with color compensation includes a control circuit that provides four output paths that can be amplified separately via one or more stages of programmable gain amplifiers and/or summing amplifiers. The control circuit allows four independent readouts for even rows, odd rows, even columns and odd columns, thus providing separate and/or simultaneous output paths for Red, Green and Blue pixels.

10 For example, one embodiment of the imaging system employs a readout control that provides outputs for the Red pixel, the Blue pixel, and the two Green pixels. Thus, the imaging system allows further gain compensation for a Green pixel that resides in an even column compared to a Green pixel that resides in an odd column. The four signals are then amplified via four corresponding programmable gain amplifiers. The readout control logic ensures that the row and column switches are closed in the appropriate sequence.

15 The present invention does not require the integrated color imaging system to employ a simultaneous readout of the n-by-n pixel block. A 'pipeline' approach may be utilized instead of a parallel readout. The pipeline approach uses one or more analog line storage units, e.g., capacitors. For example, in one embodiment using the Bayer color pattern, two line storage units are used. The first of two consecutive lines that is readout from the array is stored in the first line storage unit. The second line is averaged with the stored line to produce the RGB triplets, while a "first" line of the next two consecutive lines is readout and stored in the second line storage unit and so on. Thus, the two line storage units are used in a 'ping pong' fashion.

20 The imaging system does not restrict the type of transfer function that is implemented in the programmable gain amplifiers. Each of the four amplifiers can implement a different transfer function such as log or an exponent where the power value is programmable. Thus, each color can be optimized independently for maximum dynamic range.

25 In one embodiment of the imaging system with color compensation, the imaging system further employs several gain stages for color convolutions associated with white

balance. The imaging system employs a readout control that provides three outputs for the Red pixel, the Blue pixel, and either the even Green pixel or the odd Green pixel via a multiplexor. The three output signals are then amplified via nine programmable gain amplifiers and summed via three summing amplifiers accordingly. The readout control
5 logic ensures that the row and column switches are closed in the appropriate sequence.

Another aspect of the invention relates to a fixed pattern noise reduction apparatus and process. The fixed pattern noise reduction process reduces noise related to pixel-to-pixel variation. This variation is primarily due to dark current leakage, which may be integrated together with the signal and hence contaminate the signal. The
10 dark current leakage may be due to thermal generation in the neutral bulk material, in the depletion region and due to surface states. The dark current level may vary between pixels and may be particularly noticeable between columns due to column buffers.

The fixed pattern noise reduction process of the present invention allows increased dynamic range (high image quality), high speed of operation and reduced
15 computational complexity. The fixed pattern noise reduction of the present invention is advantageously performed in the analog domain before an analog-to-digital conversion.

In the imaging system of the present invention with fixed pattern noise reduction, the array of pixels comprises a group of exposed pixels and a group of dark pixels. In one embodiment, the dark pixels are deposited with an opaque mask layer and thus are not exposed to light. In one embodiment, the programmable readout
20 control circuit has a programmable non-destructive readout mode.

In one embodiment, the array includes a row of dark pixels. Each image pixel value is produced from a combination of an exposed pixel and a dark pixel that resides in the same column. The two pixels are read simultaneously, and the dark value is
25 subtracted from the exposed value. In another embodiment, the array includes several rows of dark pixels.

In one embodiment, the imaging system produces a black and white image. In another embodiment, the imaging system further comprises a color filter layer deposited on the exposed pixel sensor elements. In one embodiment, the color filter
30 layer comprises Red, Green, and Blue filters organized in the Bayer pattern. In another embodiment, the color filter layer comprises Yellow, Cyan and Magenta filters.

In other embodiments, other color filter systems and/or other patterns or configurations may be used. In addition, other embodiments of the imaging system do not have pixels organized in a rectangular matrix.

5 In one embodiment, at least a portion of the sensor cells are active. In another embodiment, at least a portion of the sensor cells are passive.

The imaging system in accordance with the present invention may also include additional on-chip or off-chip amplification stages, analog-to-digital conversion units, memory units and various other signal processing blocks. In one embodiment, the imaging system further comprises a micro-lenses layer.

10 In one embodiment, the imaging system further contains a control circuit that allows for special pixel readout modes and a circuit for performing an averaging and/or a subtraction operation.

15 In one embodiment, the imaging system employs an on-the-fly fixed pattern noise reduction process that subtracts dark current during the sensor readout stage. The on-the-fly fixed pattern noise reduction process is capable of reading two consecutive rows simultaneously by a readout shift register and a row readout control, re-reading a dark row together with an exposed row, subtracting a dark row value from an exposed row value with a summing amplifier and amplifying the difference with a programmable gain amplifier.

20 In another embodiment, the imaging system employs a mode of on-the-fly fixed pattern noise reduction that subtracts a dark current *average* value during the sensor readout stage. The imaging system is capable of reading three consecutive rows simultaneously by a column shift register and a row readout control, re-reading the dark rows together with an exposed row, averaging the dark rows with a summing amplifier, subtracting the averaged dark row value from the exposed row value with a summing amplifier, and amplifying the difference with a programmable gain amplifier. The imaging system utilizes several dark rows for improved quality. Each image pixel value is produced from a combination of a current exposed pixel and a dark current value that is the average of two dark pixels residing in the same column.

25 30 The present invention does not limit the number of dark rows that are averaged nor does it restrict the readout mode options. Furthermore, in other embodiments of the

present invention, the on-the-fly fixed pattern reduction can be performed with or without on-the-fly color interpolation, with or without sub-sampling, and can be further combined with a window readout mode where only a sub-region of the whole sensor array is utilized.

5 Another aspect of the present invention relates to an integrated circuit imaging system that offers on-line bad pixel correction process that can be performed in the analog domain and thus provides high speed operation.

Brief Description of the Drawings

10 Figure 1 illustrates one embodiment of an imaging system coupled to a television.

 Figure 2 illustrates one embodiment of an imaging system coupled to a computer.

 Figure 3 illustrates a Bayer pattern color filter for the primary color system.

15 Figure 4 illustrates one embodiment of a CMOS integrated circuit color imaging system that supports on-the-fly color interpolation.

 Figure 5 illustrates one embodiment of a readout sequence for the system of Figure 4 with on-the-fly color interpolation in a full resolution mode.

20 Figure 6 illustrates one embodiment of the on-the-fly color interpolation process in a full resolution mode.

 Figure 7 illustrates one embodiment of a readout sequence for on-the-fly color interpolation in a sub-sampling mode.

 Figure 8 illustrates one embodiment of a CMOS integrated circuit color imaging system that supports on-the-fly color interpolation in a sub-sampling mode.

25 Figure 9 illustrates one embodiment of the on-the-fly color interpolation process in a sub-sampling mode.

 Figure 10 illustrates a one embodiment of window mode.

 Figure 11 illustrates one embodiment of a readout control that supports on-the-fly color interpolation in a full resolution mode as shown in Figure 5.

Figure 12 illustrates one embodiment of a readout control that supports on-the-fly color interpolation in sub-sampling mode shown in Figure 8, as well as the full resolution mode shown in Figure 5.

5 Figure 13 illustrates one embodiment of a CMOS integrated circuit color imaging system with color correction.

Figure 14 provides one embodiment of a process for color correction.

Figure 15 illustrates one embodiment of a CMOS integrated circuit color imaging system with white balance.

10 Figures 16, 16A and 16B provide one embodiment of a process for white balance.

Figure 17 presents embodiments of optional transfer function for the programmable gain amplifiers.

Figures 18, 18A and 18B provide an another embodiment of the process shown in Figure 16.

15 Figure 19 illustrates another embodiment of a CMOS integrated circuit color imaging system with white balance.

Figure 20 illustrates one embodiment of an imaging system that supports fixed pattern noise reduction.

Figure 21 illustrates one embodiment of a fixed pattern noise reduction process.

20 Figure 22 illustrates another embodiment of an imaging system that supports fixed pattern noise reduction.

Figure 23 illustrates another embodiment of a fixed pattern noise reduction process.

25 Figure 24 illustrates one embodiment of a CMOS integrated circuit imaging device implementation that accommodates on-the-fly bad pixel correction.

Figure 25 illustrates a flowchart for the on-the-fly bad pixel correction of Figure 24.

Detailed Description of the Preferred Embodiments

30 The present invention relates to a novel imaging system that provides flexible addressing and processing of imaging pixel sensor elements. The novel architecture of

the present invention allows for a highly integrated, low cost imager with high speed performance and good image quality. For example, the imaging system may provide on-the-fly color interpolation, color compensation (also called color correction, color maximization or white balance) and/or fixed pattern noise reduction.

5 The exemplifying imaging systems described below with reference to Figures 1-23 use a CMOS integrated circuit, an array of pixels organized in a rectangle matrix, and a color filter with a primary color system (RGB) in a Bayer color pattern. The imaging systems of the present invention may be implemented with a charge coupled device (CCD) or other imaging technologies. Likewise, the imaging systems of the
10 present invention may be implemented with another color system, such as the complimentary color system (Yellow, Cyan and Magenta) and/or another color pattern. In addition, the imaging system of the present invention may be implemented with the pixels organized in another pixel matrix or pixel topography. For example, the array does not have to be rectangular.

15 The imaging system may also include either on-chip, as is possible with CMOS integrated circuit imaging devices, or off-chip, as is the case with CCD integrated circuit imaging devices, amplification stages, analog to digital conversion units, memory units and various other signal processing blocks. In addition, the system may further comprise a micro-lenses layer.

20 In one embodiment, the color interpolation system, the color compensation system and/or the fixed pattern noise reduction system reside together with the sensor array in the same chip, such as in a CMOS integrated circuit color imaging device. In another embodiment, the color interpolation system, the color compensation system and/or the fixed pattern noise reduction system reside in a separate companion chip,
25 such as in a CCD integrated circuit imaging device.

Figures 1 and 2 illustrate exemplifying systems incorporating the novel imaging system 100, 102. The imaging systems 100, 102 will be described in greater detail below with reference to Figures 3-23.

30 Figure 1 illustrates one embodiment of an imaging system 100 coupled to a television 116 via a coax cable 114. The exemplifying system 100 includes a lens 102, a sensor array 104 which may have color filters, a readout control 106, gain amplifiers

108 for each color, a NTSC encoder 110 including gamma correction and a power supply 112. In one embodiment, the imaging system 100 is a video camera. In other embodiments, the imaging system 100 may be implemented in security cameras, digital cameras, camcorders, video telephones and the like.

5 Figure 2 illustrates one embodiment of an imaging system 122 coupled to a computer 126 via a USB cable 124. The exemplifying system 122 includes a lens 102, a sensor array 104 which may have color filters, a readout control 106, gain amplifiers 108 for each color, an analog to digital converter 118, a USB interface 120 and a power supply 112. In one embodiment, the imaging system 122 is a video camera. In other
10 embodiments, the imaging system 122 may be implemented in security cameras, digital cameras, camcorders, video telephones and the like.

 Figure 3 illustrates a conventional Red, Green and Blue (primary color system) Bayer color pattern 130 for a color filter that is deposited on an array of pixel cells that detect light. The pattern core is a group of 2 by 2 pixels that contains 2 green
15 components 134, 136, one red component 132 and one blue component 138. The 2 green components 134, 136 are diagonal neighbors, and the red and the blue components 132, 138 are diagonal neighbors. Thus, the green resolution of the array is reduced by a ratio of 2:1 horizontally only, while the red and the blue resolution is reduced by a ratio of 2:1 horizontally and vertically. The pattern 130 exploits the fact
20 that the human eye perceives intensity edges better than color edges and that the green component contains the highest amount of intensity information.

On-The-Fly Color Interpolation

 As will now be described, an imaging system with a flexible pixel address scheme allows for on-the-fly interpolation of colors based on the outputs of two or
25 more pixels. On-the-fly color interpolation relates to color reconstruction during the sensor readout stage. Color reconstruction relates to reconstructing desired color components for each pixel in order to maintain the original unfiltered array resolution and to compensate for the fact that each filtered pixel is only capable of detecting a single color.

30 The on-the-fly color interpolation process of the present invention provides high speed of operation and reduced computational complexity with good color image

quality. The on-the-fly color interpolation process is advantageously suited for many imaging applications that do not require high color precision or high image quality, as well as those which do. For example, some high quality, digital cameras have modes of operation such as a 'preview' mode where image quality is less important than speed and implementation complexity.

One embodiment of the on-the-fly color interpolation process provides at least two modes of operation: a full resolution mode and a sub-sampling mode. Full resolution mode is preferably used when high image quality is desired. In full resolution mode, each Red-Green-Blue (RGB) triplet needed for a color pixel representation is produced from a group of 2x2 pixels within the Bayer pattern. The four pixels are read out simultaneously, the two diagonally neighboring Green pixels are summed together, and the gain associated with the Green pixels is reduced in half. The resulting Green component is sent out with the diagonally neighboring Red and Blue pixels to produce one RGB triplet. Each subsequent RGB triplet shares one of the Green pixels and either the Red or Blue pixel of the preceding RGB triplet.

Sub-sampling mode is preferably used when a lower resolution image is desired, such as a preview feature. Sub-sampling is achieved via skipping pixels along the horizontal and/or the vertical axis of the pixel array. For a sub-sampling ratio of 1:j vertically and 1:k horizontally, where j, k are even, each RGB triplet that is needed for a color pixel representation is produced from a group of j by k pixels with the Bayer pattern. All Green pixels in the j*k neighborhood are averaged to produce the green component. Similarly, all of the Red pixels in the same neighborhood are averaged to produce the Red component, and all Blue pixels in the neighborhood are averaged to produce the Blue component. The three components are then sent out as the RGB triplet representing the j by k group of pixels. The sub-sampling process can be achieved by reading the j rows in parallel or in series.

Both the full resolution and the sub-sampling modes of operation can be further combined with a window readout mode (also called "window mode" or "windowing"). In window mode, a sub-region of the whole pixel sensor array is readout and processed. Thus, a window mode is essentially a cropping operation that produces a smaller area of interest. Window readout mode is faster and provides a higher frame rate. Window

mode may be used in digital cameras for exposure and focus calculations, for electronic zoom and more. Window mode is described in greater detail below with reference to Figure 10.

Figure 4 illustrates one embodiment of a novel CMOS integrated circuit color imaging system 140 that supports on-the-fly color interpolation using analog signals. The system 140 uses the Bay color pattern illustrated in Figure 3. As illustrated in Figure 4, the system 140 includes a column readout control circuit 146, a line synchronization signal 142, a pixel clock 144, a first column readout line 148, a second column readout line 148', a third column readout line 148'', a first switch 150, a first column buffer 152, a second switch 150', a second column buffer 152', an analog summing amplifier 154, a programmable analog red gain amplifier 156, a red video out line 158, a red gain control line 160, a green video out line 162, a green gain control line 164, a programmable analog green gain amplifier 166, a blue video out line 168, a blue gain control line 170, a programmable analog blue gain amplifier 172, a red output path 174, a green output path 176, a blue output path 178, a row readout control circuit 180, a frame synchronization line 182, a line synchronization line 184, a first row readout line 186, a second row readout line 186', a first row buffer 188, a second row buffer 188', a first red pixel 190, a first green pixel 192, a second green pixel 194 and a first blue pixel 196.

In the description herein, a "programmable" component refers to a component that responds to a command from an end-user of the imaging system or to a command issued by internal firmware according to firmware stored in the imaging system. For example, if an end-user chooses a 'zoom' function or a 'preview' function on a video camera containing the imaging system of the present invention, the imaging system directs the programmable components to act in a predefined manner according to firmware stored in the imaging system.

The imaging system of the present invention does not need the color gain amplifiers 156, 166, 172 (Figure 4) to be implemented as a separate stage. In one embodiment, a plurality of color gain amplifiers are contained within the pixel circuitry of the sensor array. In another embodiment, a plurality of color gain amplifiers are contained within the column buffers 152, 152'.

As will now be described, the system 140 accommodates on-the-fly color interpolation via a programmable pixel readout mode. The exemplifying system 140 implements an RGB Bayer color pattern on-the-fly color interpolation when windowing and sub-sampling are not active. The system 140 is not limited in its mode of operation and can support windowing and sub-sampling via the programmable readout control circuitry 146, 180, the summing amplifier(s) 154 and the programmable gain amplifiers 156, 166, 172.

Figure 5 illustrates one embodiment of a pixel readout sequence for the system 140 of Figure 4 with on-the-fly color interpolation in a full resolution mode. The sequence accommodates an RGB Bayer pattern color filter 130 (Figure 3) in a non-window mode and without sub-sampling. Each RGB triplet that is needed for a color pixel representation is produced from a group of 2x2 pixels that contains the Bayer pattern core. For example, while reading four pixels substantially simultaneously, the two diagonally neighboring Green pixels 192, 194 are averaged and sent out with the neighboring Red and Blue pixels 190, 196 to produce a RGB triplet. Three other subsequent RGB triplet shares one of the Green pixels 192, 194 and either the Red or the Blue pixels 190, 196 with the previous RGB triplet. For example, in Figure 5, four RGB triplets are formed from a 3x3 pixel block 200:

$$\{R(0,0), [(G(1,0) + G(0,1))/2], B(1,1)\}$$

$$\{R(2,0), [(G(1,0) + G(2,1))/2], B(1,1)\}$$

$$\{R(0,2), [(G(0,1) + G(1,2))/2], B(1,1)\}$$

$$\{R(2,2), [(G(2,1) + G(1,2))/2], B(1,1)\}$$

where the first numeral in the parenthesis represents the row and the second numeral represents the column.

Similar readout sequences can be devised in accordance with the present invention for color filter patterns other than Bayer and for color systems other than the primary one.

Figure 6 illustrates one embodiment of the on-the-fly color interpolation process in a full resolution mode. In a process block 202, the illustrated system 140 may simultaneously read out a group of 2 by 2 pixels that contains the Bayer pattern core. In a process block 203, the system 140 may perform several acts substantially simultaneously (in parallel). In blocks 204, 210, the system 140 reads the

corresponding red and the blue components 190, 196 that reside in two consecutive columns 148, 148" (Figure 4) and amplifies accordingly via the programmable red and blue gain amplifiers 156, 172. In blocks 206-208, the system 140 reads the two green components 192, 194 that reside in two consecutive columns 148, 148" and sums the values with the summing amplifier 154. The gain from the summing amplifier 154 is adjusted accordingly via the programmable gain amplifier 166. The programmable readout control 146, 180 ensures that the appropriate switches are closed to allow the correct readout sequence as described in Figure 5.

In Figure 6, the acts in block 203 (amplifying and outputting a red value, amplifying and outputting a green value and amplifying and outputting a blue value) are performed substantially simultaneously. In another embodiment, the acts of block 203 are performed in a sequence, e.g. the system 140 amplifies and outputs a red value, then amplifies and outputs a green value, and then amplifies and outputs a blue value.

In Figure 6, the system 140 advances to the next column in a block 212, new COLUMN = old COLUMN + 1. In a block 214, the system 140 determines whether the column readout control 146 is exceeding the last Red pixel in a row. If yes, then the process proceeds to a block 216, and the row readout control 180 advances to the next row, new ROW = old ROW + 1. If not, then the process loops back to block 202. In a block 218, the system determines whether the row readout control 180 is exceeding the last Red pixel in a frame. If yes, then the process stops in a stop block 220 and waits for further commands. If not, then the process proceeds to block 202.

Figure 7 illustrates one embodiment of a readout sequence for on-the-fly color interpolation in a sub-sampling mode. In Figure 7, the sequence accommodates an RGB Bayer pattern color filter 230 in a non-window mode with sub-sampling. In Figure 7, the sub-sampling ratio is 1:4 horizontally and 1:4 vertically. Each RGB triplet that is needed for a color pixel representation is produced from a group 232 of 4x4 pixels that contains 4 Bayer pattern cores. The 8 green pixels are averaged to produce the green component, the 4 red pixels are averaged to produce the red component, and the 4 blue pixels are averaged to produce the blue component. Specifically, as illustrated in Figure 7, the red component comprises

$$[(R(0,0) + R(2,0) + R(0,2) + R(2,2))/4],$$

the green component comprises

$$[(G(1,0) + G(3,0) + G(0,1) + G(2,1) + G(1,2) + G(3,2) + G(0,3) + G(2,3))/8],$$

and the blue component comprises

$$[(B(1,1) + B(3,1) + B(1,3) + B(3,3))/4]$$

- 5 Similar readout sequences can be devised for color filter patterns other than Bayer and for color systems other than the primary one.

Figure 8 illustrates one embodiment of a CMOS integrated circuit color imaging system 240 that supports on-the-fly color interpolation in a programmable pixel readout mode, such as a sub-sampling mode. The structure of the system 240 is substantially similar to the system 140 of Figure 4, except that the system 240 also includes a red summing amplifier 242 and a blue summing amplifier 244. The function of these additional amplifiers is described below. Figure 8 presents an implementation for an RGB Bayer pattern on-the-fly color interpolation where windowing is not active and sub-sampling is active. However, the system 240 is not limited to a Bayer pattern and/or the primary color scheme. Nor is the system 240 limited in its mode of operation. The system 240 can be realized to support both window and sub-sampling via the programmable readout control circuitry 146, 180, the summing amplifier(s) 242, 154, 244, and the programmable gain amplifiers 156, 166, 172.

Figure 9 illustrates one embodiment of the on-the-fly color interpolation process in a sub-sampling mode, as described with reference to Figures 7 and 8. Figure 9 illustrates sub-sampling a RGB Bayer color filter 230 (Figure 7) using a ratio of 4:1 horizontally and 4:1 vertically. In a block 250, a group 232 (Figure 7) of 4 by 4 pixels that contains Bayer pattern cores is read out simultaneously.

In a process block 253, the system 240 may perform several acts substantially simultaneously (in parallel). In blocks 252, 254, the four red pixels shown in sub-sample 232 of Figure 7 are summed and amplified by the red amplifiers 242, 156 of Figure 8. In blocks 256, 258, the 8 green pixels that reside in four consecutive columns (Figure 7) are summed via the green summing amplifier 154 and amplified by the green amplifier 166 (Figure 8). In blocks 260, 262, the four blue pixels shown in sub-sample 232 of Figure 7 are summed and amplified by the blue amplifiers 244, 172 of Figure 8. The programmable readout control 146, 180 of Figure 8 ensures that the appropriate

switches are closed to allow the correct readout sequence as described in Figures 7 and 9.

In Figure 9, the acts in block 253 are performed substantially simultaneously. In another embodiment, the acts of block 253 are performed in a sequence, e.g. the system 240 sums, amplifies and outputs a red value, then sums, amplifies and outputs a green value, and then sums, amplifies and outputs a blue value.

In Figure 9, the system 240 advances to the next 4x4 block horizontally in a block 264, new COLUMN = old COLUMN + 4. In a block 266, the system 240 determines whether the column readout control 146 is exceeding the last 4x4 block in a row. If yes, then the process proceeds to a block 268, and the system 240 advances vertically to the next 4x4 block, new ROW = old ROW + 4. If not, then the process loops back to block 250. In a block 270, the system 240 determines whether the row readout control 180 is exceeding the last 4x4 block in a frame. If yes, then the process stops in a stop block 272 and waits for further commands. If not, then the process proceeds to block 250.

Figure 10 illustrates a one embodiment of window readout mode. For simplicity, sub-sampling and/or on-the-fly color interpolation are not included in the embodiment shown in Figure 10. In window mode, a sub-region 280 of the pixel array exposed area 130 is readout. In the embodiment shown in Figure 10, the pixel array exposed area size is n by m, the window size is chosen to be n - 4 by m - 6, and the window origin is chosen to be (4,4). Thus, the sub-region 280 comprises pixels in a rectangle defined by four pixels R(4,4), G(m-3,4), G(4,n) and B(m-3,n) at the four corners.

A window mode is essentially a cropping operation that produces a smaller area of interest. The readout is faster and provides a higher frame rate than the system 240 of Figure 8. The system 240 of Figure 8 may be modified to support window readout mode. Window mode may be used in digital cameras for exposure and focus calculations, for electronic zoom and more.

Figure 11 illustrates one embodiment of a column readout control 146 (Figure 4) that supports on-the-fly color interpolation in a full resolution mode as illustrated in Figure 5. The readout control of the system 146 advantageously allows the

simultaneous readout of a 2x2 pixel block. The readout control comprises a column readout control 146 that provides simultaneous readout of two columns and a row readout control 180 that provides a simultaneous readout of two rows.

The column readout control 146 includes a shift register that is responsible for closing the switches of the column buffers two at a time. The pixel clock 144 clocks the shift register 146. The line sync signal 142 is feeding the shift register 146 and is multiplied by two to allow signal width of two consecutive bits. Thus, the shift register 146 closes two consecutive column buffer switches coupled to lines 148, 148' simultaneously.

The row readout control 180 (Figure 4) is substantially similar except the shift register clock of the row readout control 180 utilizes a line sync 184 instead of the pixel clock, and the shift register input data utilizes a frame sync 182 instead of the line sync signal.

Figure 12 illustrates one embodiment of a novel readout control that supports on-the-fly color interpolation in sub-sampling mode shown in Figure 8, as well as the full resolution mode shown in Figure 5. Figure 12 demonstrates the column readout control 146. The sub-sampling modes chosen for the example are: 1:2, 1:4, 1:8 and 1:16. The readout control of Figure 12 also supports overlap such as the case in the full resolution mode (Figure 5). The shift register that is responsible for closing the column buffer switches is divided into 16-bit registers 318, 318', 318" that are clocked by the pixel clock 324.

In Figure 12, each register 318 is loaded with a bit pattern that is produced by the pattern generator 290. In a full resolution mode, the pattern generator 290 shifts a pattern 292 (provided by the initial pattern signal line) left by 1 during each cycle and causes an overlap. For a sub-sampling ratio of 1:4, "1111" is the pattern 292 provided on an initial pattern line and loaded since four columns are read simultaneously. In each cycle, the pattern is shifted left and selected by the multiplexors 304, 308. For example, a shift amount of 4 is used for sub-sampling 1:4 without overlap. The down counter 314 is responsible for counting pixel clocks for each 16-bit register 318, e.g. for sub-sampling of 1:4 without overlap, the counter 314 counts 4 times from the line sync 322. Then the counter 314 is reloaded by the register 312, and the next 16-bit register

318' is enabled by the latch 316 and the initial pattern is reloaded by the 16-bit register 308.

The row readout control 180 is similar to the column readout control 146 shown in Figure 12 except the clock 324 utilizes a line sync 184 instead of the pixel clock, and the initializing signal 322 utilizes a frame sync 182 instead of the line sync signal.

Color Compensation

As previously discussed, another aspect of the invention relates to color compensation (correction or maximization). The color compensation process compensates for differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials, temperature or manufacturing. The color compensation process of the present invention improves color dynamic range, decreases computations and hardware and improves speed of operation. The color compensation process of the present invention is advantageously performed in the analog domain before an analog-to-digital conversion.

Figure 13 illustrates one embodiment of a CMOS integrated circuit color imaging system 330 of the present invention with analog color correction. The system 330 provides a programmable pixel readout mode that allows four independent readouts and four programmable gain amplifiers 156, 172, 342, 352 for amplifying the four output paths (red, blue, even green, odd green) separately. Figure 13 presents an implementation for an RGB Bayer pattern. However, the system 330 is not limited to a Bayer pattern and/or the primary color scheme. In Figure 13, the system 330 employs readout control circuitry 146, 334 with separate paths for even and odd rows and columns 174, 178, 348, 350, and programmable gain amplifiers 156, 172, 342, 352. Thus, the system 330 provides four separate, simultaneous output paths with potentially different amplified gains.

The system 330 is not restricted to a particular type of transfer function with respect to the programmable gain amplifiers 156, 172, 342, 352. In one embodiment, each of the four programmable gain amplifiers 156, 172, 342, 352 implement different transfer functions, such as a log or an exponent function where the power value is programmable, as shown in Figure 17. Thus, the different transfer functions advantageously allow different levels of color compensation for different colors. In one

embodiment, the transfer functions may be modified in real-time according to the level of compensation needed to accommodate temperature, differences in the response of various color filters and variations within the integrated circuit sensor array, such as process, materials or manufacturing. In another embodiment, the transfer functions may be pre-set at the manufacturer to accommodate variations within the integrated circuit sensor array, such as process, materials or manufacturing.

Figure 14 provides one embodiment for the analog color correction process performed by the system 330 of Figure 13. In a block 360, the system 330 (Figure 13) reads a pixel value. In a block 363, the system 330 may perform several acts simultaneously (in parallel). Blocks 362, 368 and 372 determine the color of the pixel value. In a block 364, the red pixel 190 that resides in an even column and even row is amplified via the red programmable amplifier 156. In a block 366, the green pixel 192 that resides in an even column and odd row is amplified via the even green programmable amplifier 342. In a block 370, the green pixel 194 that resides in an odd column and even row 194 is amplified via the odd green amplifier 352. In a block 374, the blue pixel 196 that resides in an odd column and odd row is amplified via the blue programmable amplifier 172. The acts in block 363 are performed substantially simultaneously. In another embodiment, the acts of block 363 are performed in a sequence.

In a block 376, the system 330 advances to the next column, new COLUMN = old COLUMN + 1. In a block 378, the system 330 determines whether the system readout is exceeding the last pixel in a row. If not, the system 330 returns to process block 360. If yes, the system 330 advances to the next row, new ROW = old ROW + 1, in a block 380. In a block 382, the system 330 determines whether the system readout is exceeding the last row in a frame. If not, the system 330 returns to process block 360. If yes, the system 330 stops in a stop block 384 and waits for further commands.

In addition to the significant innovations described above, one embodiment of the color compensation process of the present invention also improves white balancing, which is used to compensate colors for different illumination temperatures.

Figure 15 illustrates one embodiment of a CMOS integrated circuit color imaging system 390 that accommodates analog white balance with programmable pixel

readout modes, multiplexor(s) 418, programmable gain amplifiers 398-414, and summing amplifiers 392, 394 and 396. Figure 15 presents an implementation for an RGB Bayer pattern. However, the system 390 is not limited to a Bayer pattern and/or the primary color scheme. In Figure 15, the system 390 employs readout control circuitry 146, 180 with separate paths for even and odd rows 186 and columns 148, a multiplexor 418 for selecting the appropriate green path, programmable gain amplifiers 398-414, and summing amplifiers 392, 394 and 396. The multiple amplifier gain stages provide convolutions associated with white balance.

Figures 16, 16A and 16B (hereinafter referred as "Figure 16") provide one embodiment of an analog white balance process performed by the system 390 of Figure 15. In a block 420, the system 390 reads a 2x2 pixel block. In a process block 423, the system 390 may perform several acts substantially simultaneously (in parallel). In blocks 422 and 430, the system 390 determines the colors of the pixels. In blocks 424-428, the red pixel 190 is amplified by 3 red programmable amplifiers 398-402 (Figure 15). In blocks 440, 447 and 444, the blue pixel 196 is amplified by 3 blue programmable amplifiers 410-414. In a block 432, the green pixel 192 that resides in an even column and odd row is multiplexed by the multiplexor 418 with the green pixel 194 that resides in an odd column and even row to produce one green value that is amplified by 3 green amplifiers 404-408. In blocks 446, 448 and 450, each of the amplified red components is summed with the corresponding amplified green and amplified blue components via 3 summing amplifiers 392, 394 and 396 (Figure 15), and thus producing new red, green and blue components that are results of RGB convolutions.

In a block 452, the system 390 advances to the next column, new COLUMN = old COLUMN + 1. In a block 454, the system 390 determines whether the system readout is exceeding the last pixel in a row. If not, the system 390 returns to process block 420. If yes, the system 390 advances to the next row, new ROW = old ROW + 1, in a block 456. In a block 458, the system 390 determines whether the system readout is exceeding the last row in a frame. If not, the system 390 returns to process block 420. If yes, the system 390 stops in a stop block 460 and waits for further commands.

The acts in block 423 are performed substantially simultaneously. For example, the decision blocks 422 and 430 may be performed in parallel by reading two or more pixels simultaneously. As another example, blocks 424, 426, 428, may be performed in parallel by themselves or with blocks 440, 447, 444 and/or blocks 434, 436, 438. In other embodiments, the blocks may be performed in a sequence. The system 390 may further comprise storage circuits to store the values of the amplified red, green and blue components before they are summed in blocks 446, 448 and 450.

Figure 17 presents embodiments of optional transfer functions 470, 472, 474, such as an exponent transfer function, for the programmable gain amplifiers 398-414 of Figure 15. Each amplifier can implement a different transfer function and thus optimize each color for maximum dynamic range.

Figures 18, 18A and 18B (hereinafter referred as "Figure 18") provide another embodiment of the process shown in Figure 16. The process of Figure 18 provides white balance and on-the-fly color interpolation. The process may be performed by the system 390 of Figure 19. The process of Figure 18 is similar to the process shown in Figure 16, except the two green pixels are averaged by a summing amplifier 482 (Figure 19) in a block 432 of Figure 18. In Figure 18, like the process in Figure 16, some of the process blocks are performed in parallel. In other embodiments, the blocks may be performed in a sequence.

Figure 19 is another embodiment of a CMOS integrated circuit color imaging system 390 of the present invention with white balance. The system 390 of Figure 19 is similar to the system 390 of Figure 15, except the system 390 of Figure 19 comprises a summing amplifier 482 instead of a multiplexor 418 in Figure 15. The system 390 of Figure 19 provides white balance and on-the-fly color interpolation.

Fixed Pattern Noise Reduction

Another aspect of the invention relates to a fixed pattern noise reduction apparatus and process. The fixed pattern noise reduction process reduces noise related to pixel-to-pixel variation. This variation is primarily due to dark current leakage, which may be integrated together with the signal and hence contaminate the signal. The dark current leakage may be due to thermal generation in the neutral bulk material, in

the depletion region and due to surface states. The dark current level may vary between pixels and may be particularly noticeable between columns due to column buffers.

The fixed pattern noise reduction process of the present invention allows increased dynamic range (high image quality), high speed of operation and reduced computational complexity. The fixed pattern noise reduction of the present invention is advantageously performed in the analog domain before an analog-to-digital conversion.

Figure 20 illustrates one embodiment of an imaging system that supports fixed pattern noise reduction. Specifically, Figure 20 illustrates one embodiment of a CMOS integrated circuit color imaging system 500 that supports on-the-fly fixed pattern noise reduction. In the illustrated embodiment, additional circuitry is not needed for post-processing in order to provide the fixed pattern noise reduction. The system 500 comprises a column readout shift register 146, a row readout shift register 180, a dark row readout control or path 492, a row of dark pixel sensor elements (dark row) 490, a first row of exposed pixel sensor elements 186, a second row of exposed pixel sensor elements 186', a summing amplifier 496, a programmable gain amplifier 498 and a plurality of switches 508.

In one embodiment, the dark pixels are deposited with an opaque mask layer and thus are not exposed to light. A row of pixels with dark pixels may be referred to as a "dark row." The system 500 presents an implementation for a red/green/blue (RGB)(primary color scheme) in a Bayer pattern with on-the-fly fixed noise reduction when windowing and sub-sampling are not active.

The system 500, however, is not limited to a Bayer pattern and/or the primary color scheme. Other embodiments may use other color schemes and/or other color patterns. Nor is the system 500 limited in its mode of operation. For example, the system 100 of Figure 1 may be modified to support windowing and/or sub-sampling.

In Figure 20, two pixels in the same column are read out simultaneously in response to signals from the column shift register 146, the row shift register 180 and the dark row readout control 492. One pixel is read from the dark row 490 and another pixel is read from the first exposed row 186. The dark pixel value is then subtracted from the exposed pixel value by the summing amplifier 496, thereby providing fixed pattern noise reduction. Additional gain is applied to the new value by the

programmable gain amplifier 498. The dark row 490 may be re-used for each exposed row 186, 186'. The programmable readout control components 146, 180 ensure that the appropriate switches 508 are closed to allow the correct readout sequence.

Figure 21 illustrates one embodiment of a fixed pattern noise reduction process that may be performed by the system 500 of Figure 20. Specifically, Figure 21 illustrates one embodiment of an on-the-fly fixed pattern noise reduction process utilizing a single dark row 190. In Figure 21, in a process block 520, the system 500 reads two pixels in a current column: a dark pixel in the dark row 490 and an exposed pixel in an exposed row 186. In a block 522, the summing amplifier 496 subtracts a value associated with the dark pixel from a value associated with the exposed pixel. In a block 524, the system 500 clips the difference found in block 522 to zero if the difference is negative. In a block 526, the system 500 advances to the next column of the system 500 in Figure 20, new COLUMN = old COLUMN + 1.

In a decision block 528, the system 500 determines whether the column shift register 146 has reached the last pixel in a row 186. If the column shift register 146 has not reached the last pixel in a row 186, then the system 500 returns to process block 520 to process the next column. If the column shift register 146 has reached the last pixel in a row 186, then the system 500 advances to the next row 186' in a process block 530, new ROW = old ROW + 1. In a decision block 532, the system 500 determines whether the row shift register 180 has reached the last row in a frame of pixel sensor elements. If the row shift register 180 has not reached the last row in a frame of sensor elements, then the system 500 returns to process block 520 to process the first column in the next row 186'. If the row shift register 180 has reached the last row in the frame, then the system 500 may wait for a further command in an end block 534.

Figure 22 illustrates another embodiment of an imaging system 540 that supports fixed pattern noise reduction. Specifically, Figure 22 illustrates one embodiment of a CMOS integrated circuit color imaging system 540 that supports on-the-fly fixed pattern noise reduction with two dark rows. The imaging system 540 uses more than one dark rows for improved quality. Each image pixel value is preferably produced from a combination of a current exposed pixel and a dark current value that is the average of two dark pixels residing in the same column.

In Figure 22, the system 540 comprises a column readout shift register 146, a row readout shift register 180, a dark row readout control or path 492, a first row of dark pixel sensor elements (first dark row) 490, a second row of dark pixel sensor elements (second dark row) 544, a first row of exposed pixel sensor elements 186, a second row of exposed pixel sensor elements 186', a first summing amplifier 542, a second summing amplifier 496, a programmable gain amplifier 498 and a plurality of switches 508. The system 540 presents an implementation for a red/green/blue (RGB)(primary color scheme) in a Bayer pattern with on-the-fly fixed noise reduction when windowing and sub-sampling are not active.

In another embodiment, the dark rows 490, 544 and/or individual dark pixels are distributed over the imaging array.

The system 540 is not limited to a Bayer pattern and/or the primary color scheme. Other embodiments may use other color schemes and/or other color patterns. Nor is the system 540 limited in its mode of operation. For example, the system 540 of Figure 22 may be modified to support window and sub-sampling.

In Figure 22, three pixels in the same column are read out simultaneously by the column shift register 146, the row shift register 180 and the dark rows readout path 492. Two pixels are read from the two dark rows 490, 544 and a third pixel is read from the first exposed row 186. The two dark pixels are then averaged by the first summing amplifier 542 to produce an average dark value. The average dark value is then subtracted from the exposed pixel by the second summing amplifier 496. Additional gain is applied to the new value by the programmable gain amplifier 498. The dark row 490 is re-used for each exposed row 186. The programmable readout control components 146, 180 ensure that the appropriate switches 508 are closed to allow the correct readout sequence.

In Figure 22, the system 540 has two dark rows 490, 544 for producing average dark values. In other embodiments, there are more than two dark rows which are averaged. The fixed pattern noise reduction system of the present invention is not limited to two dark rows nor to any other particular number. The system 540 in Figure 22 can be modified to average any number of dark rows prior to the subtraction from the exposed pixel by the summing amplifier 496.

Figure 23 illustrates one embodiment of an on-the-fly fixed pattern noise reduction process utilizing multiple dark rows 490, 544. The process of Figure 23 may be performed by the system 540 of Figure 22. In Figure 23, in a process block 550, the system 540 reads three pixels in a current column: a dark pixel from each of the two dark rows 490, 544 and an exposed pixel in an exposed row 186. In a process block 552, the first summing amplifier 552 averages the values associated with the two dark pixels. In a process block 554, the second summing amplifier 496 subtracts the averaged dark pixel value from a value associated with the exposed pixel. In a process block 546, the system 540 clips the difference found in block 554 to zero if the difference is negative. In a process block 558, the system 540 advances to the next column.

In a decision block 560, the system 540 determines whether the column shift register 146 has reached the last pixel in a row 186. If the column shift register 146 has not reached the last pixel in a row 186, then the system 540 returns to process block 550 to process the next column. If the column shift register 146 has reached the last pixel in a row 186, then the system 540 advances to the next row 186' in a process block 562. In a decision block 564, the system 540 determines whether the row shift register 180 has reached the last row in a frame of pixel sensor elements. If the row shift register 180 has not reached the last row in a frame of sensor elements, then the system 540 returns to process block 550 to process the first column in the next row 105'. If the row shift register 180 has reached the last row in the frame, then the system 540 may wait for a further command in an end block 566.

Bad Pixel Correction

In one embodiment, the imaging system contains a signal processing circuit 624 that allows bad pixel correction as shown in Figure 24. Figure 24 demonstrates an example of a CMOS integrated circuit imaging device implementation that accommodates on-the-fly bad pixel correction. The illustration presents an implementation for a monochrome on-the-fly bad pixel correction when windowing and sub-sampling are not active. However, the present invention is not limited to a monochrome imager, nor is limited in its mode of operation and can be realized to support window and sub-sampling.

In the embodiment shown in Figure 24, a monochrome imaging system 600 employs a CMOS integrated circuit. The bad pixel correction system may be applied to CCD integrated circuits and/or different color filters.

Figure 24 illustrates one embodiment of a CMOS integrated circuit imaging system 600 that accommodates on-the-fly bad pixel correction. In Figure 24, the system 600 comprises a row shift register 180, a column shift register 146, buffers 188, 188', 152, row control lines 186, 186', column control lines 602, 602', 602'', a delay 604, a multiplexer 606, an amplifier 608, a video out line 610, an external memory control 612, a row comparator 616, a column comparator 614, an AND gate 622, a row comparator 618, a column counter 620, a row control line 630 and a column control line 632. Other circuit configurations may be implemented in accordance with the present invention. In another embodiment of Figure 24, a pipeline delay of two or more pixels is utilized. In a pipeline approach described below, a delay is not needed because one or more lines are stored such that the previous pixels are readily available for bad pixel correction.

In Figure 24, the row control line 630 inputs the total number of rows into the row counter 618, and the column control line 620 inputs the total number of columns into the column counter 620. The color imaging system 600 provides an on-the-fly bad pixel correction process that is performed during the analog sensor readout stage. The signal processing circuit 624 identifies the addresses of the bad pixels via a list stored in an external memory accessed by the external memory control 612 and corrects any bad pixels on-the-fly. The list may be stored in a memory either on-chip or off-chip.

Figure 25 illustrates a flowchart for the on-the-fly bad pixel correction of Figure 24. The detection of bad pixels is performed off-line and a bad pixel list is stored in an external memory which is accessed by the external memory control 612. The correction process utilizes the list and replaces a defect pixel with its adjacent neighbor.

In a block 630 of Figure 25, the circuit 600 reads consecutive horizontal pixels and amplifies the pixel readouts with an amplifier 608. The delay 604 provides a temporary pixel value storage. In a block 632, the row address comparator 616 and the column address comparator 614 compare the readout pixel address from the row and column counters 618, 620 with the stored list of defective pixel addresses. In a decision

block 634, the circuit 624 determines if the current pixel is a bad one. If the comparison is positive, the output of the AND gate is 1, and the current pixel is replaced by the previous adjacent pixel that is stored in the delay 604, as shown in a block 636. If the comparison is negative, the output of the AND gate is 0, and the column shift register 146 advances to the next column in a block 638. The blocks 640-646 are substantially similar to the blocks 214-220 in Figure 6 described above.

The on-the-fly bad pixel correction embodiment may be combined with various readout modes such as windowing and sub-sampling, and additional signal processing such as on-the-fly color interpolation. The bad pixel correction system of the present invention is not limited to monochrome imaging systems and is applicable to integrated circuit color imaging systems as well. The color imaging system may utilize any color filter scheme such as the primary color system (RGB) in a Bayer pattern, a complementary color system or others. The imaging system may also use a non-rectangle matrix of pixels. A similar implementation can provide on-the-fly bad pixel correction for color imaging systems and/or different pixel topography via modification to the readout control, the pixel neighborhood size and configuration. For example, a color imaging system with an RGB Bayer pattern may use 3 horizontally consecutive pixels, i.e., pipeline delay of 3 pixels and 2 registers for temporary storage. So each color component when defective, can be replaced by the corresponding pixel with the same color component.

In other embodiments of the systems illustrated in Figures 4, 8, 13,15, 19, 20, 22, the systems may further include one or more rows and/or columns of capacitors to read and store pixel sensor values to accommodate serial readout of pixels. Using capacitors to store values reduces the number and complexity of the lines (buses) coupled the pixel sensor elements. The size of the pixel sensor elements, the size of the sensor array, the space on the chip and the placement of the components are design choices of the manufacturer.

The present invention does not require the integrated color imaging system to employ a simultaneous readout of the n-by-n pixel block. A 'pipeline' approach may be utilized instead of a parallel readout. The pipeline approach uses one or more analog line storage units, e.g., capacitors. For example, in one embodiment using the Bayer

color pattern, two line storage units are used. The first of two consecutive lines that is readout from the array is stored in the first line storage unit. The second line is averaged with the stored line to produce the RGB triplets, while a "first" line of the next two consecutive lines is readout and stored in the second line storage unit and so on.

5 Thus, the two line storage units are used in a 'ping pong' fashion.

The invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiment is to be considered in all respects only as illustrative and not restrictive and the scope of the invention is, therefore, indicated by the appended claims rather than the foregoing description. All
10 changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

WHAT IS CLAIMED:

1. A color imaging system providing on-the-fly color interpolation using analog signals to reconstruct colors during sensor readout, the imaging system
5 comprising:

an array of pixel sensor elements;

a color filter including a plurality of color filter components organized in a predefined pattern, the color filter overlaying at least a portion of the array;

a readout control circuit coupled to the array; and

10 an array controller coupled to the array, wherein the readout circuit and the array controller reconstruct color components for at least a portion of the array while the readout control circuit is reading at least said portion of the array.

2. The system of Claim 1, further comprising:

15 a comparator circuit adapted to compare an address of a pixel sensor element currently being read by the readout control circuit with a stored list of defective pixel sensor addresses; and

at least one delay element for storing at least one previous analog pixel value read by the readout control circuit, wherein if the address of the current pixel sensor element matches a defective pixel address in the stored list, the readout control circuit reads the previous analog pixel value.
20

3. The system of Claim 1, wherein the readout control circuit is adapted to read a plurality of pixel sensor elements in parallel.

4. The system of Claim 1, further comprising:

25 a first analog line storage unit, the first analog line storage unit being adapted to store a first line readout from the array; and

a second analog line storage unit, the second analog line storage unit being adapted to store a third line readout from the array, wherein the readout control circuit averages a second consecutive line readout from the array with the first line readout stored in the first analog line storage unit to produce a first red-green-blue (RGB) triplet, the readout control circuit averaging a fourth
30

consecutive line readout from the array with the third line readout stored in the second analog line storage unit to produce a second RGB triplet.

5. The system of Claim 4, wherein the analog storage units are capacitors.

6. The system of Claim 1, wherein the readout control circuit is
5 programmable to read a first pixel element in a first mode and to read a second pixel element in a second mode.

7. The system of Claim 1, wherein the pixel sensor elements form a portion of a charge coupled device.

8. The system of Claim 1, wherein the pixel sensor elements form a portion
10 of a complementary metal oxide semiconductor device.

9. The system of Claim 1, further comprising a first programmable gain amplifier adapted to amplify a first color readout signal a first amount and a second programmable gain amplifier adapted to amplify a second color readout signal a second amount.

10. The system of Claim 9, wherein the programmable gain amplifiers are
15 implemented as a separate stage.

11. The system of Claim 9, wherein the programmable gain amplifiers are contained within a pixel circuitry of the array.

12. The system of Claim 9, wherein the programmable gain amplifiers are
20 within a plurality of column buffers.

13. The system of Claim 9, wherein the programmable gain amplifiers have different transfer functions.

14. The system of Claim 1, wherein at least a portion of the pixel sensor elements are active.

15. The system of Claim 1, wherein at least a portion of the pixel sensor elements are passive.
25

16. The system of Claim 1, wherein at least a first pixel sensor element is associated with a different color filter component than a neighboring pixel sensor element.

17. The system of Claim 1, wherein the predefined pattern is a Bayer color
30 configuration.

18. The system of Claim 1, wherein the predefined pattern comprises the colors of red, blue and green.

19. The system of Claim 1, wherein the predefined pattern comprises the colors of yellow, cyan and magenta.

5 20. The system of Claim 1, further comprising a micro-lenses layer.

21. The system of Claim 1, wherein the readout control circuit and the array controller process a first set of pixel sensor elements and then process a second set of pixel sensor elements, such that the second set of pixel sensor elements overlaps a portion of the first set of pixel sensor elements.

10 22. The system of Claim 1, wherein the readout control circuit and the array controller process a first set of pixel sensor elements and then process a second set of pixel sensor elements, such that the second set of pixel sensor elements does not overlap the first set of pixel sensor elements.

15 23. The system of Claim 1, wherein the readout control circuit and the array controller process a first set of pixel sensor elements, skip a second set of pixel sensor elements and process a third set of pixel sensor elements.

24. The system of Claim 1, wherein the readout control circuit and the array controller only processes a sub-region of the array of pixel sensor elements.

20 25. The system of Claim 1, further comprising a television coupled to said readout control circuit.

26. The system of Claim 1, further comprising a personal computer coupled to said readout control circuit.

27. The system of Claim 1, further comprising a monitor coupled to said readout control circuit.

25 28. The system of Claim 1, further comprising a camera coupled to said readout control circuit.

29. A method of interpolating color components of an array of pixel sensor elements, said method comprising:

reading a portion of an array of pixel sensor elements; and

30 reconstructing color components for at least a portion of the array while said portion of the array is being read.

30. The method of Claim 29, further comprising:

comparing an address of a pixel sensor element currently being read by a readout control circuit with a stored list of defective pixel sensor addresses; and

5 storing at least one previous analog pixel value read by the readout control circuit, wherein if the address of the current pixel sensor element matches a defective pixel address in the stored list, the readout control circuit reads the previous analog pixel value.

31. The method of Claim 29, wherein reconstructing color components is performed in real-time.

10 32. The method of Claim 29, wherein reconstructing color components is performed in an analog domain.

33. The method of Claim 29, wherein the act of reading includes reading a first set of pixel sensor elements and then reading a second set of pixel sensor elements, such that the second set of pixel sensor elements overlaps a portion of the first set of pixel sensor elements.

34. The method of Claim 29, wherein the act of reading includes reading a first set of pixel sensor elements and then reading a second set of pixel sensor elements, such that the second set of pixel sensor elements does not overlap a portion of the first set of pixel sensor elements.

20 35. The method of Claim 29, wherein the act of reading includes reading a first set of pixel sensor elements, skipping a second set of pixel sensor elements and reading a third set of pixel sensor elements.

36. The method of Claim 34, further comprising:

25 summing a plurality of values associated with a plurality of pixel sensor elements associated with a first color to produce a first color component; and

summing a plurality of values associated with a plurality of pixel sensor elements associated with a second color to produce a second color component.

37. The method of Claim 29, wherein the act of reading includes reading only a sub-region of the array of pixel sensor elements.

30 38. A color imager comprising:

a first light sensor which generates a first analog output signal related to the amount of a first color of light sensed;

a second light sensor which generates a second analog output signal related to the amount of said first color of light sensed; and

5 an interpolation circuit configured to receive said first output signal and said second output signal, wherein said interpolation circuit provides an interpolation signal on the fly based on at least said first analog output signal and said second analog output signal.

10 39. A method of interpolating a color value in the analog domain in real-time, comprising:

receiving a first analog signal corresponding to the output of a first pixel element in an imager, the first pixel element used to sense light intensity of a first color;

15 receiving a second analog signal corresponding to the output of a second pixel element in the imager, the second element spaced from the first pixel element, wherein the second pixel element is used to sense light intensity of the first color; and

20 generating an analog interpolation signal, the analog interpolation signal used to recreate a color value in real-time for a location situated between the first and second pixel elements based on the first analog signal and the second analog signal.

40. The method as defined in Claim 39, further comprising generating an image based on at least the first analog signal, the second analog signal, and the analog interpolation signal.

25 41. The method as defined in Claim 39, further comprising:

reading a third pixel element located in a line of pixel elements;

skipping a fourth pixel element located in the line of pixel elements; and

reading a fifth pixel element located in the line of pixel elements.

42. The method as defined in Claim 39, further comprising performing a
30 windowing operation by reading only a subset of pixel elements during a read operation of the imager.

METHOD AND APPARATUS FOR COLOR INTERPOLATION

Abstract of the Disclosure

5 An imaging method and system that flexibly accesses light sensor elements and processes imaging signals. The imaging system comprises an array of pixel sensor cells, an array controller and a readout control circuit. The imaging system provides color interpolation.

10

H:\DOCS\ACC\ACC-1404.DOC
121299

11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
220

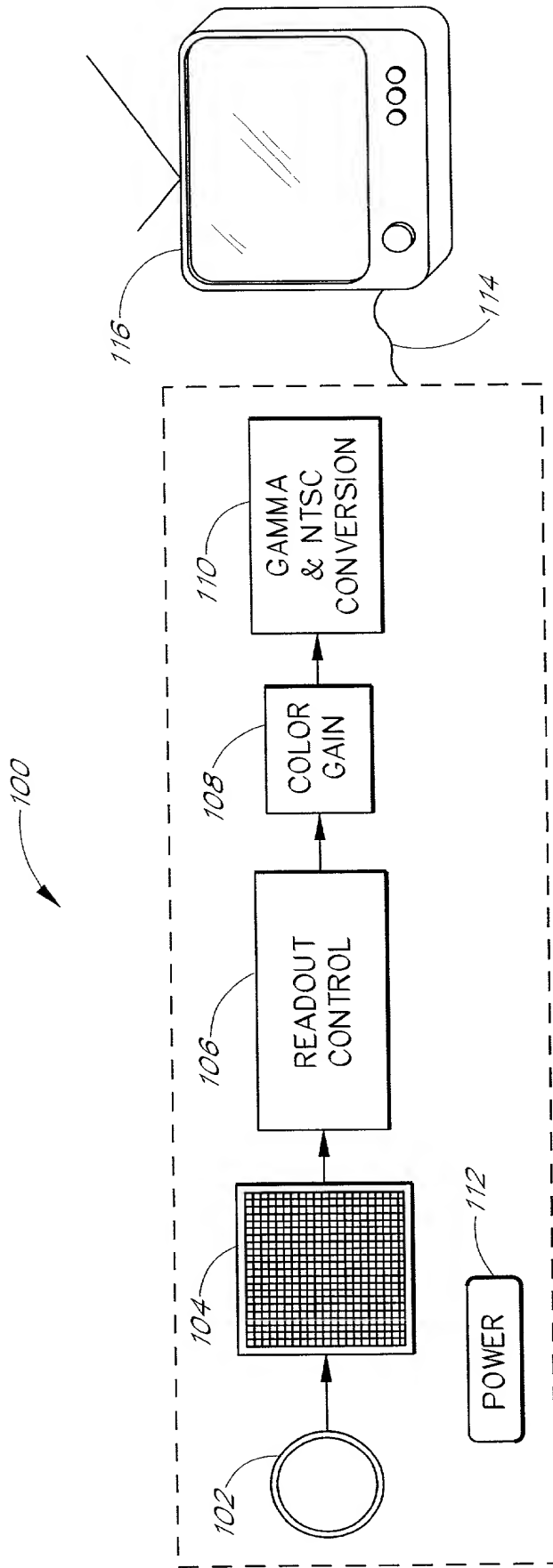


FIG. 1

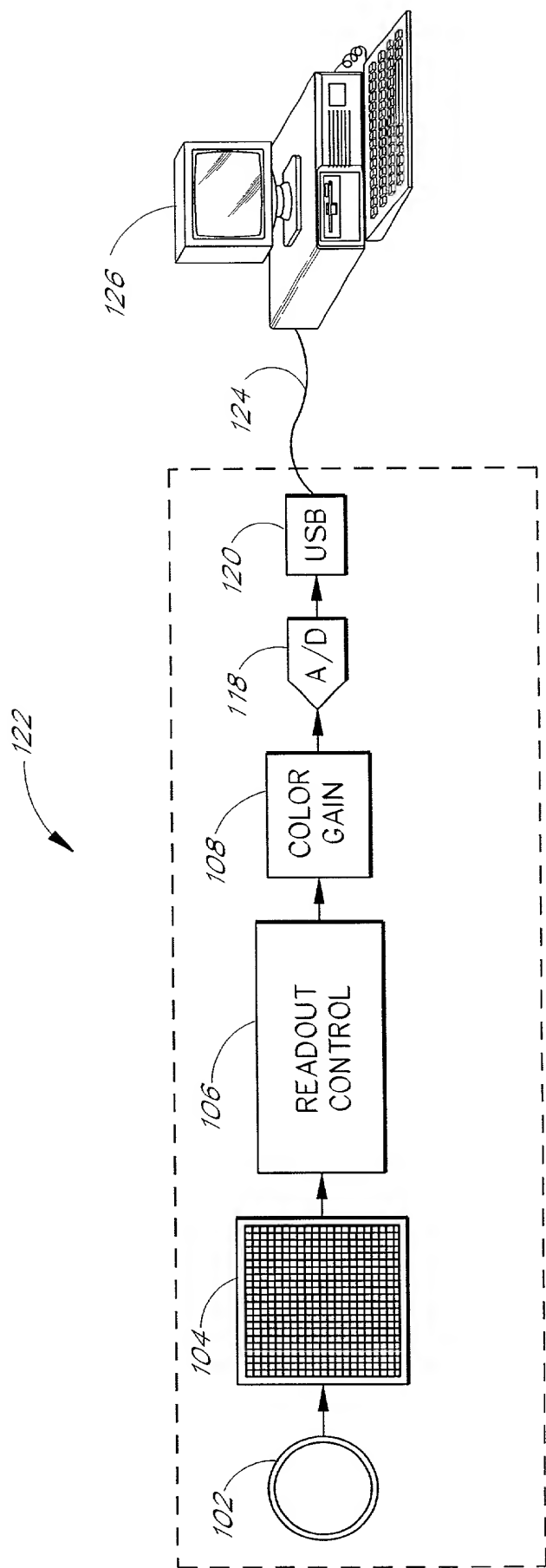


FIG. 2

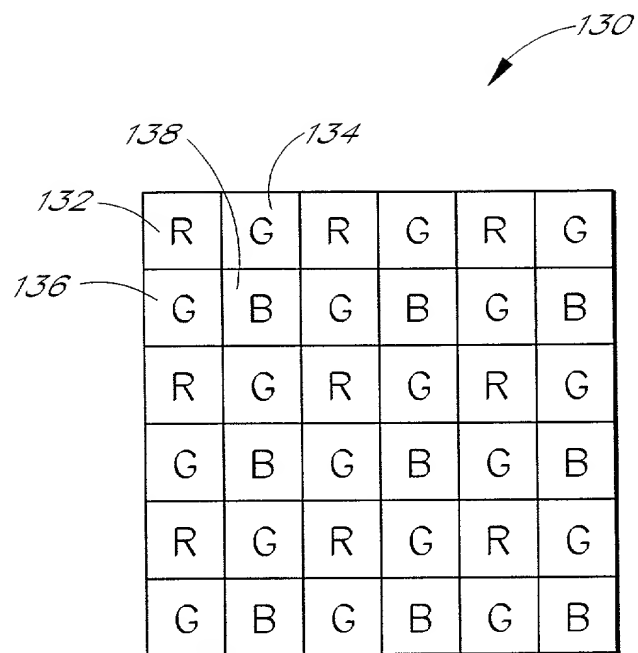


FIG. 3

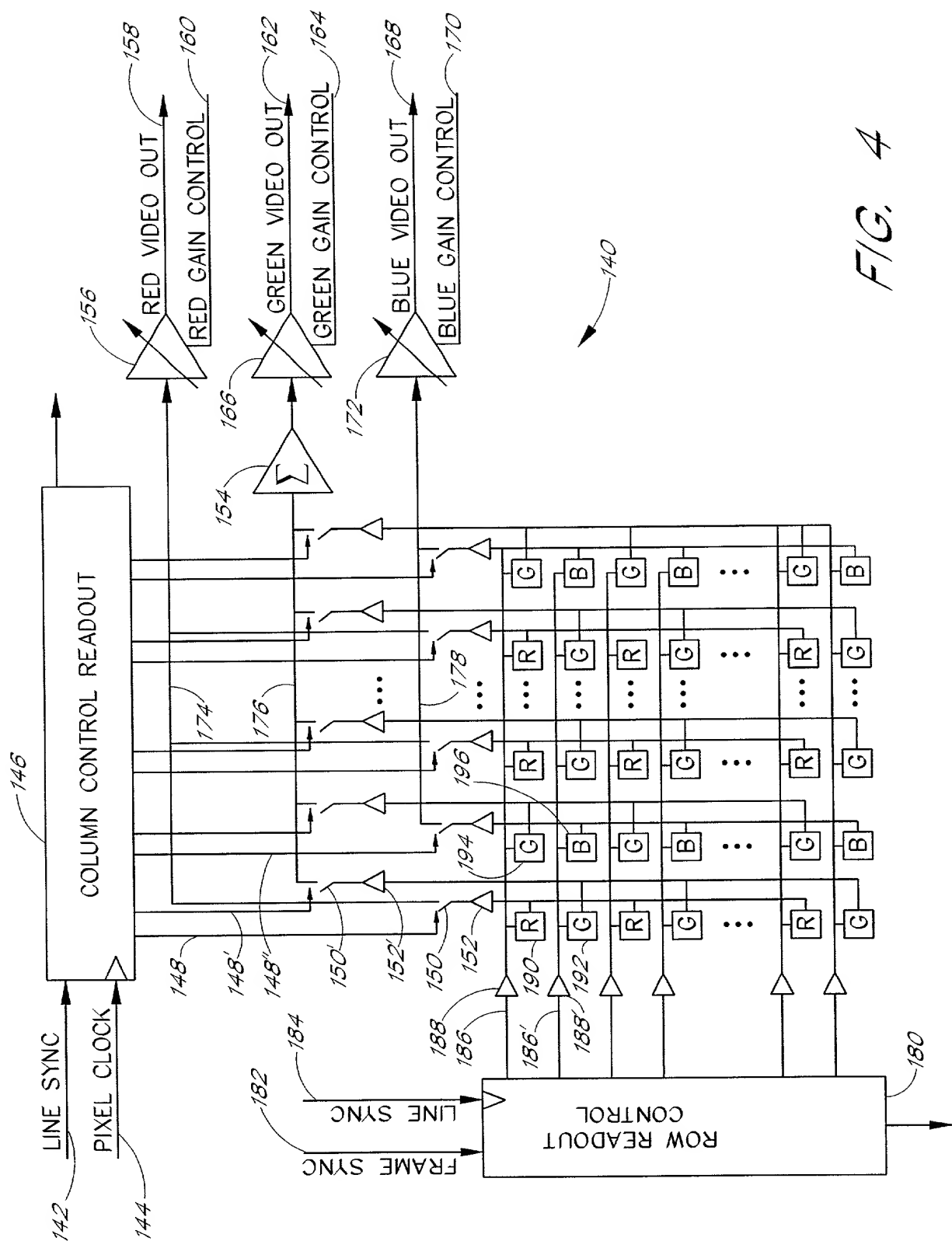


FIG. 4

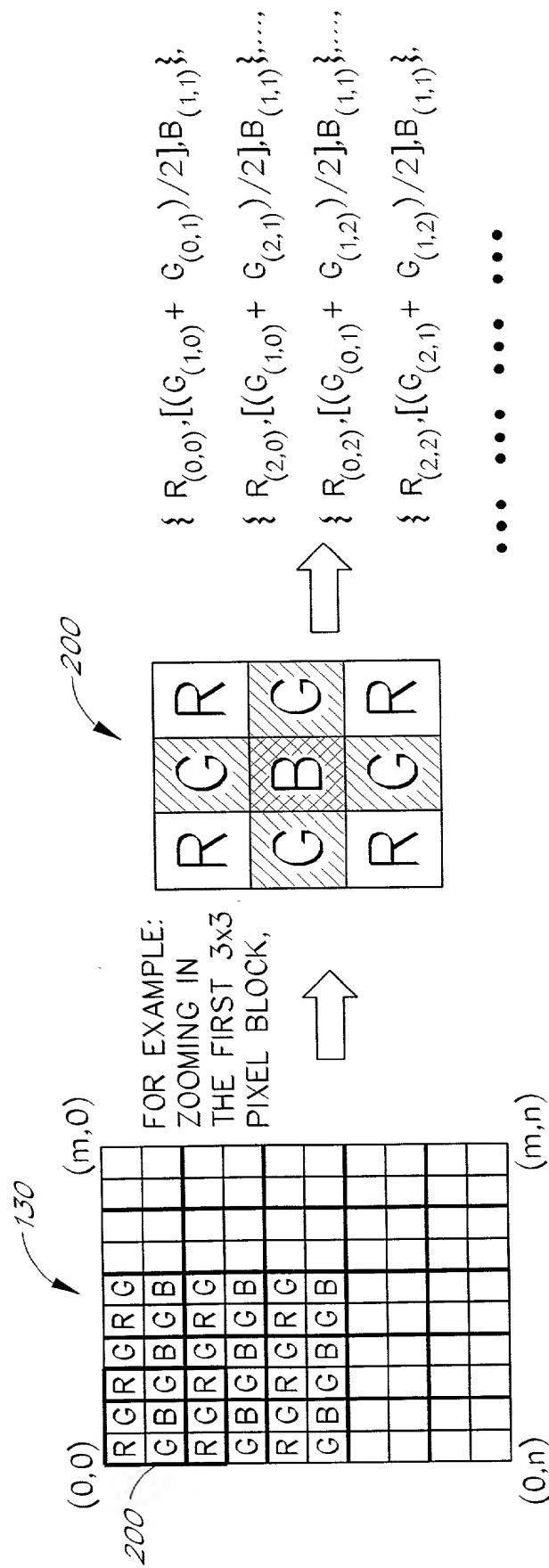


FIG. 5

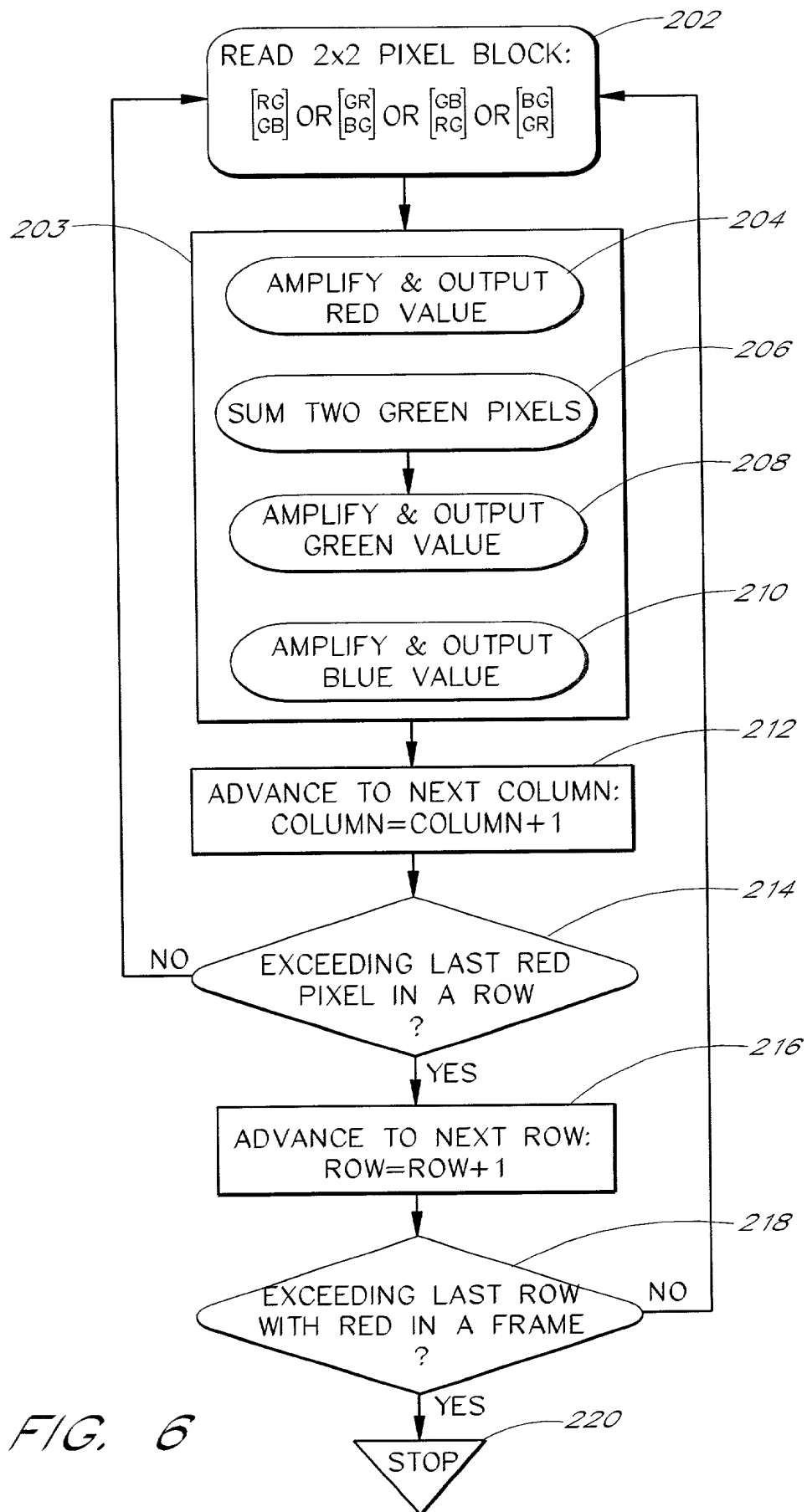


FIG. 6

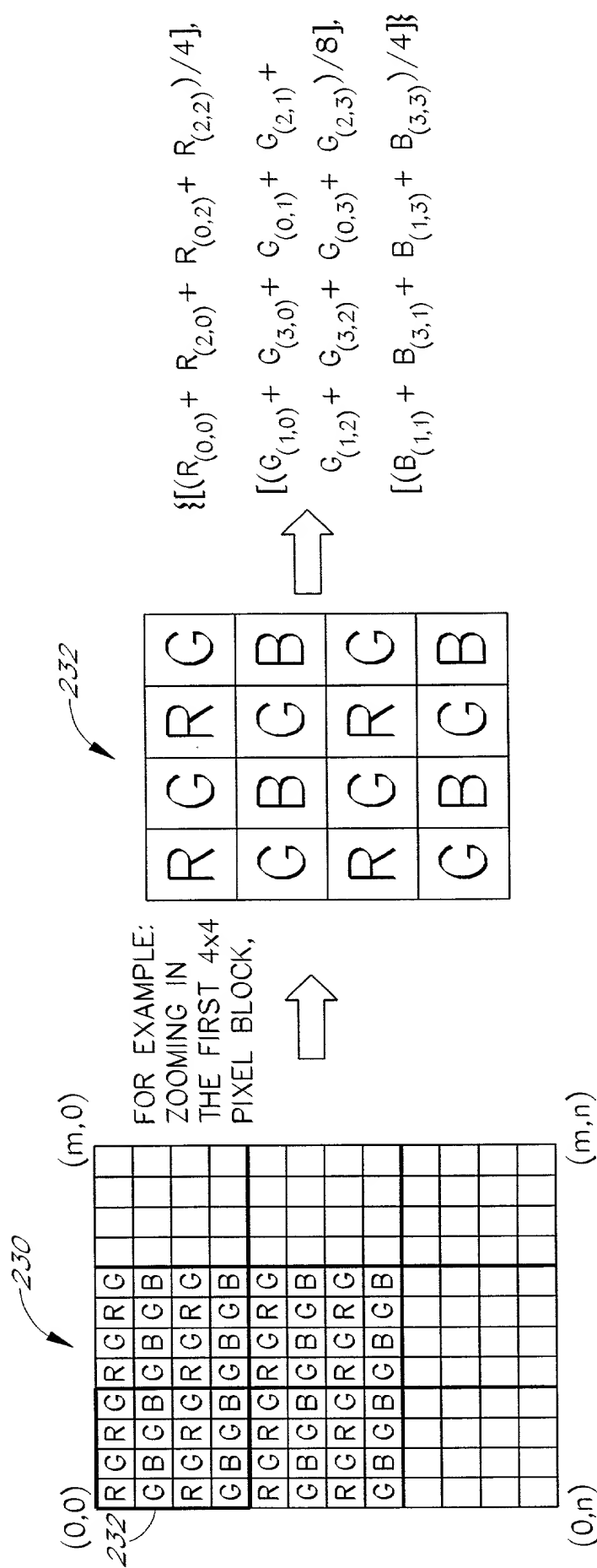


FIG. 7

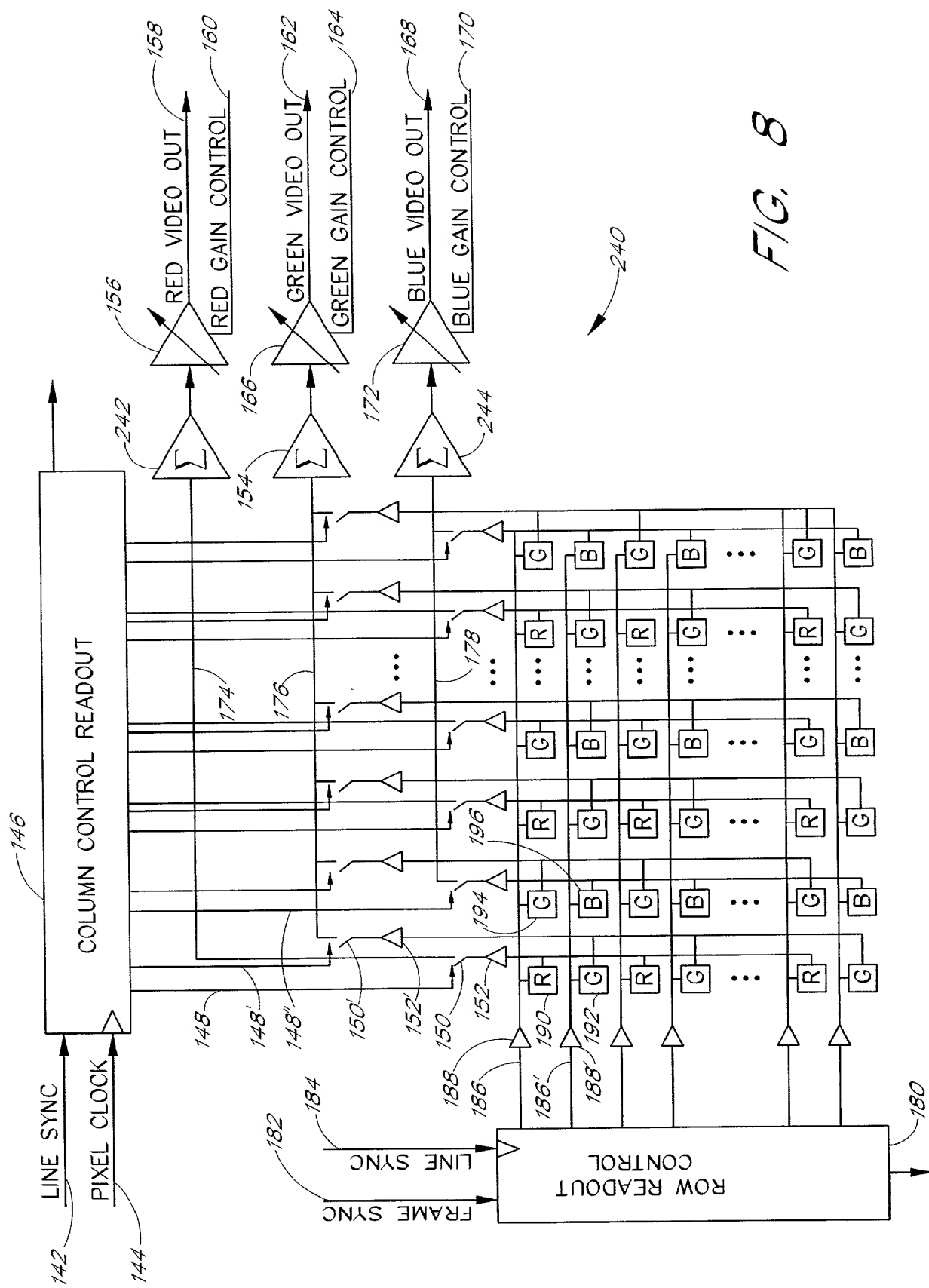


FIG. 8

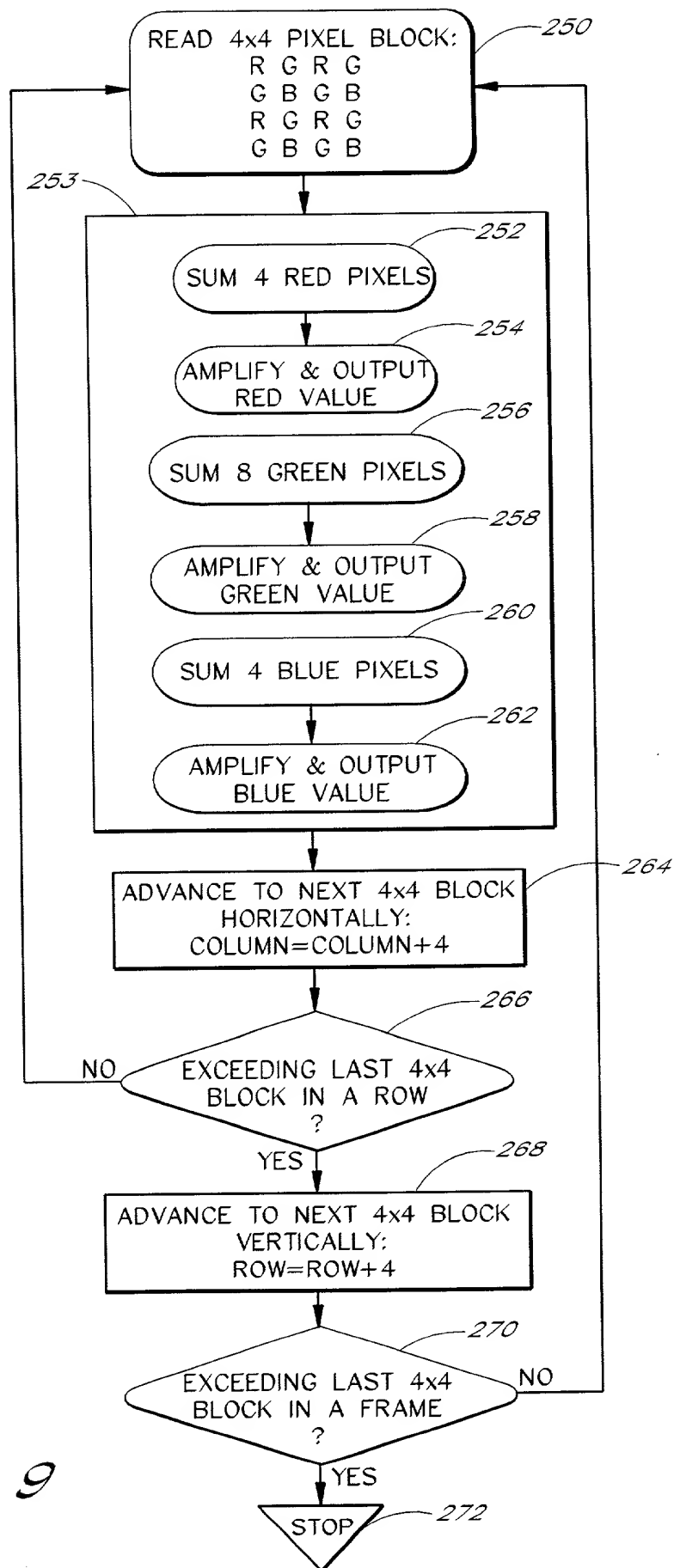


FIG. 9

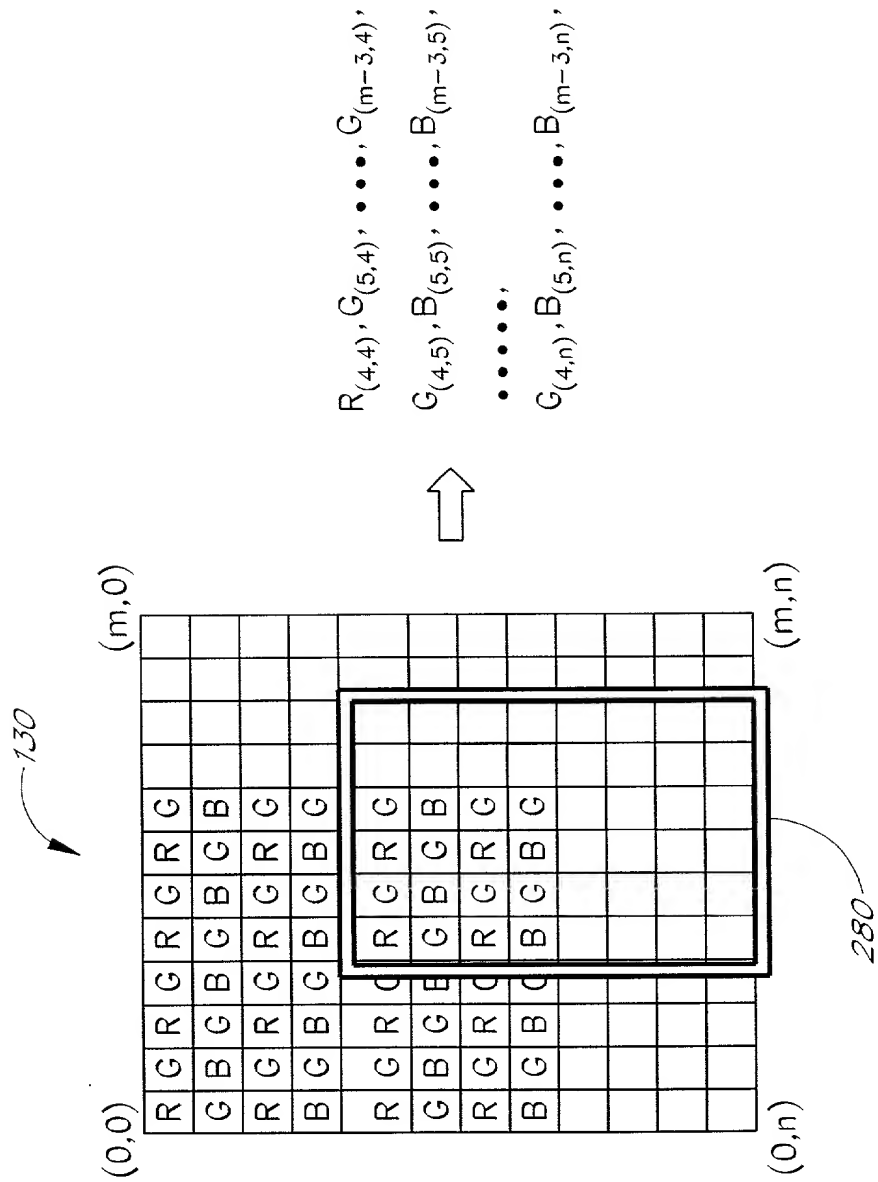


FIG. 10

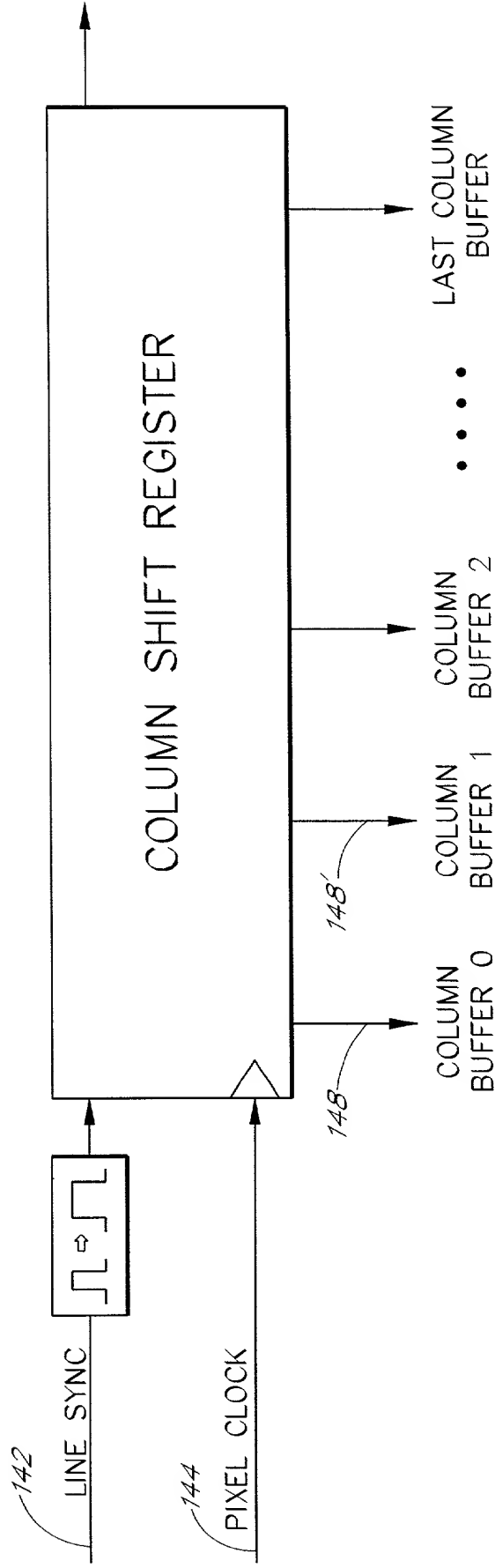
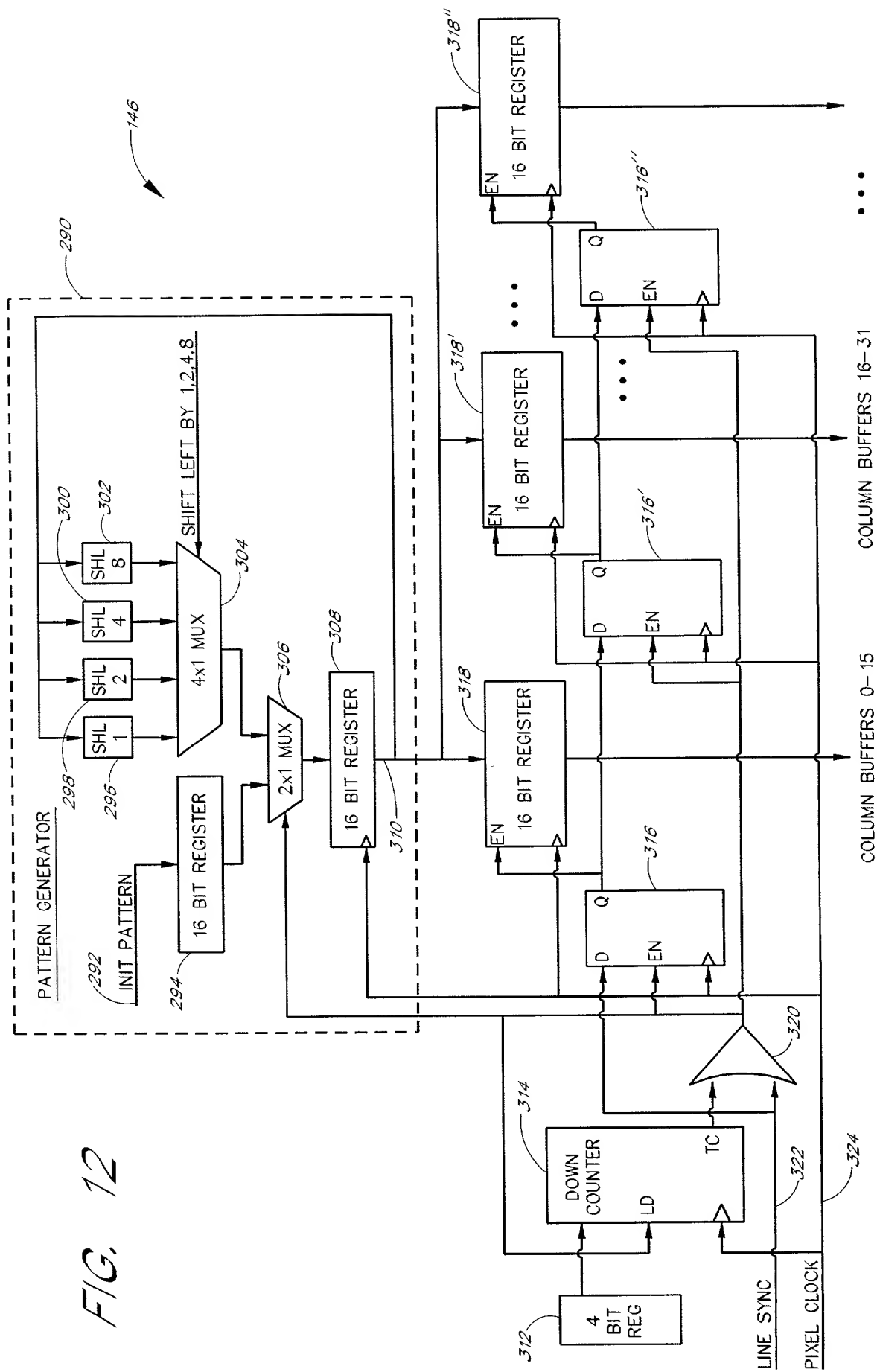


FIG. 11

[illegible]

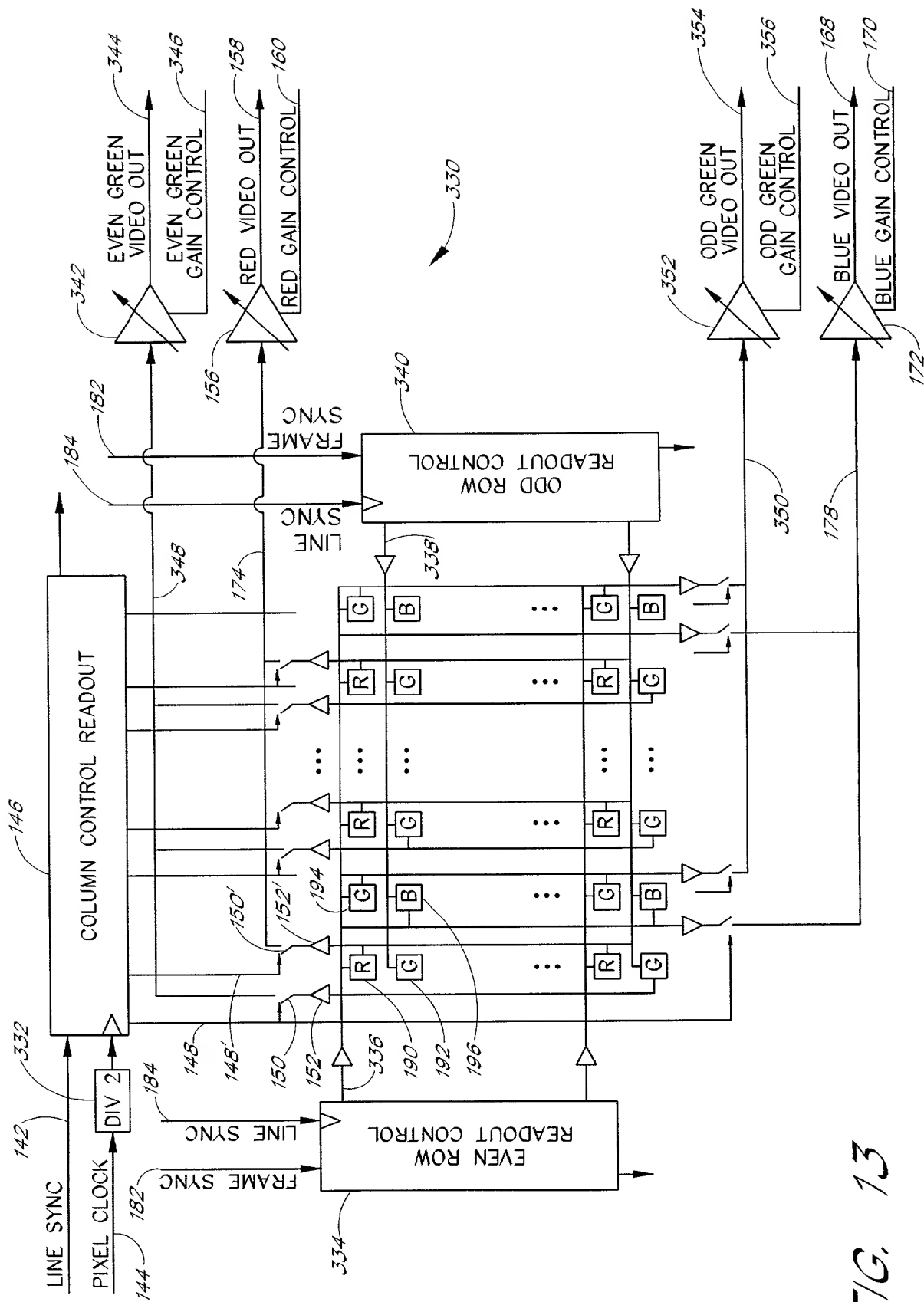


FIG. 13

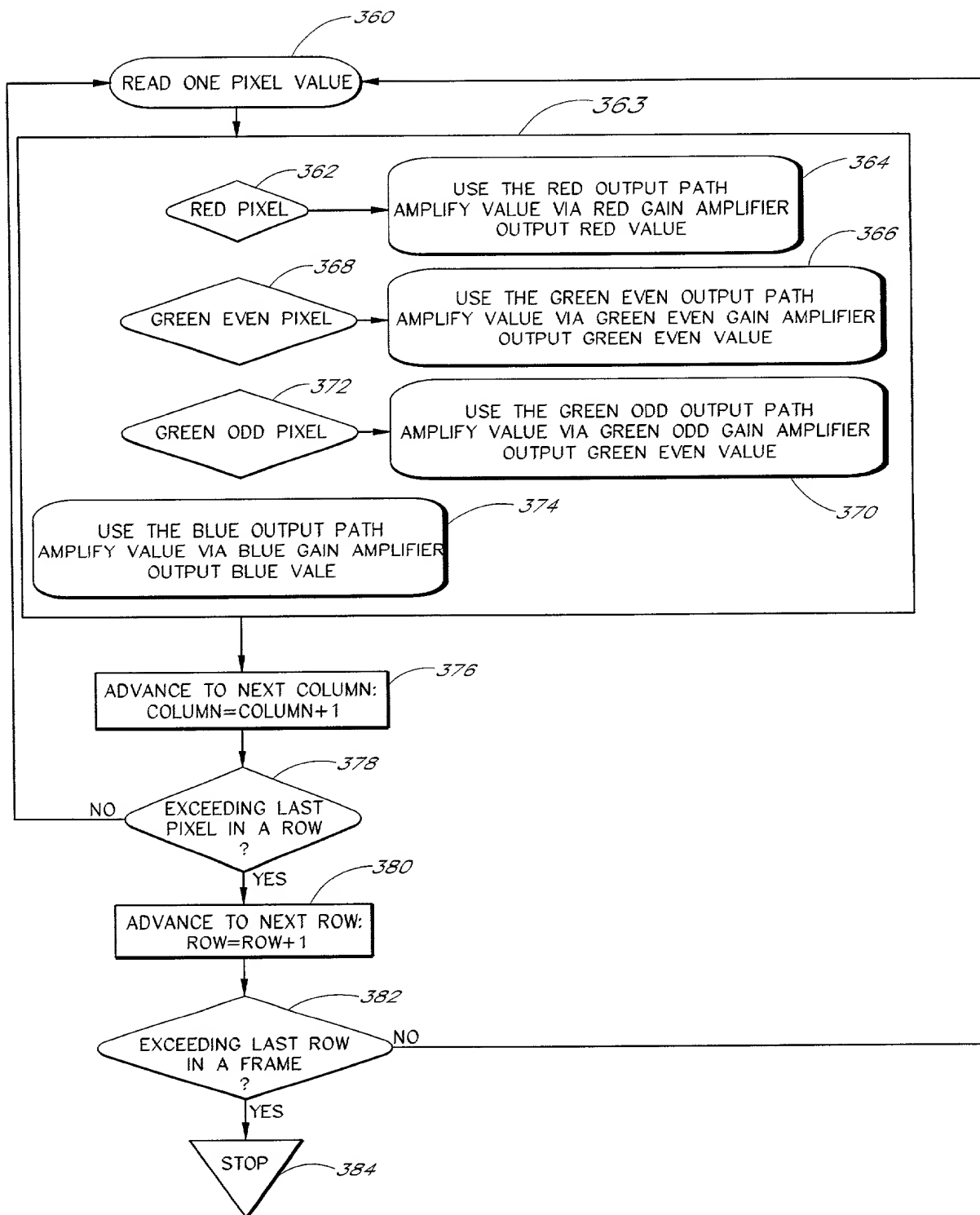


FIG. 14

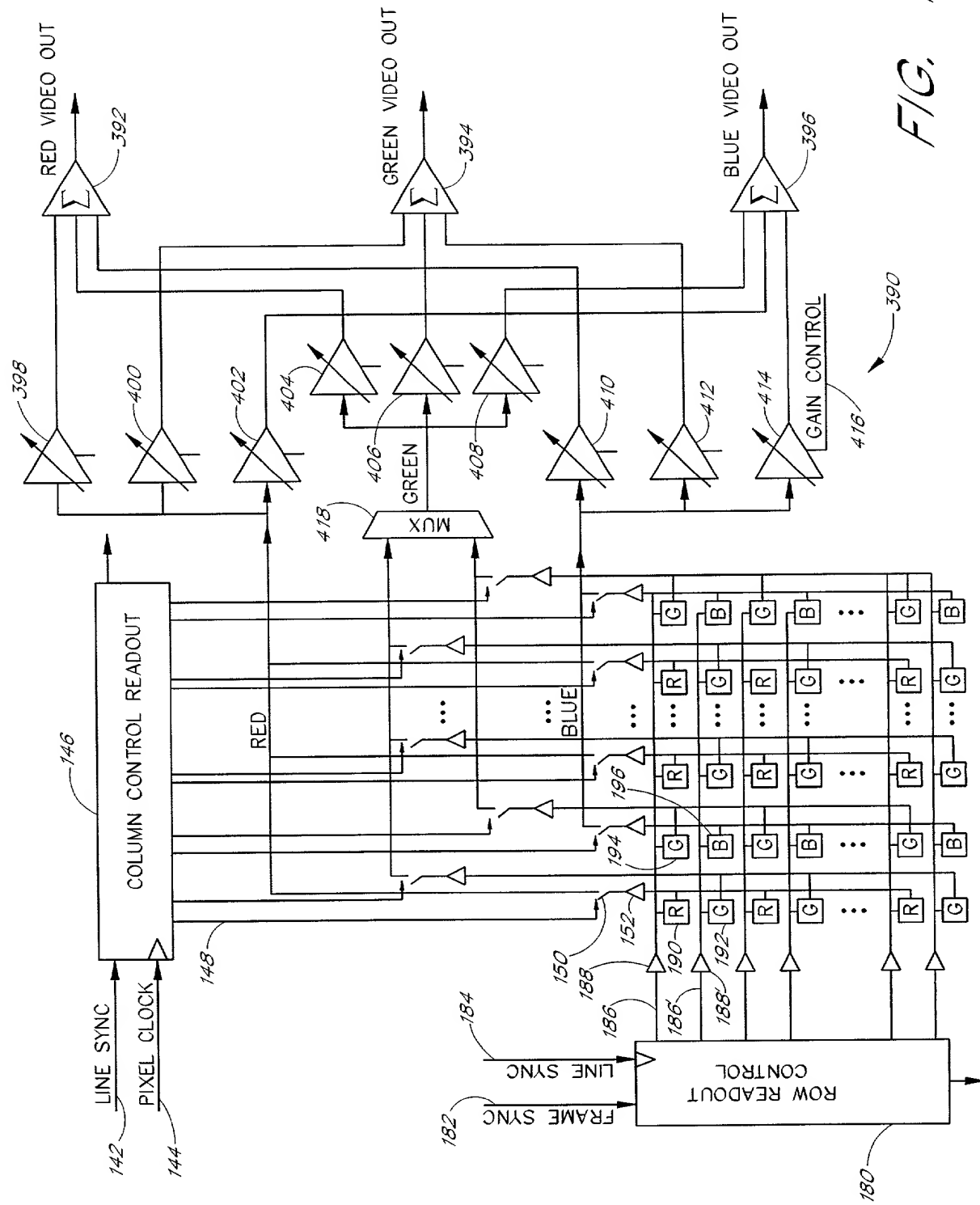


FIG. 15

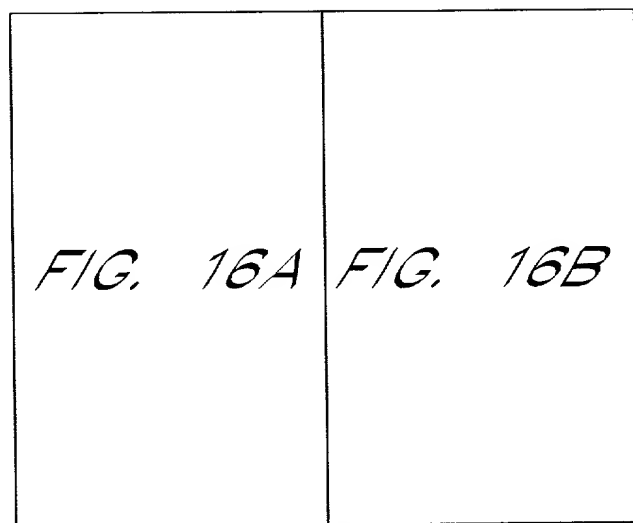


FIG. 16

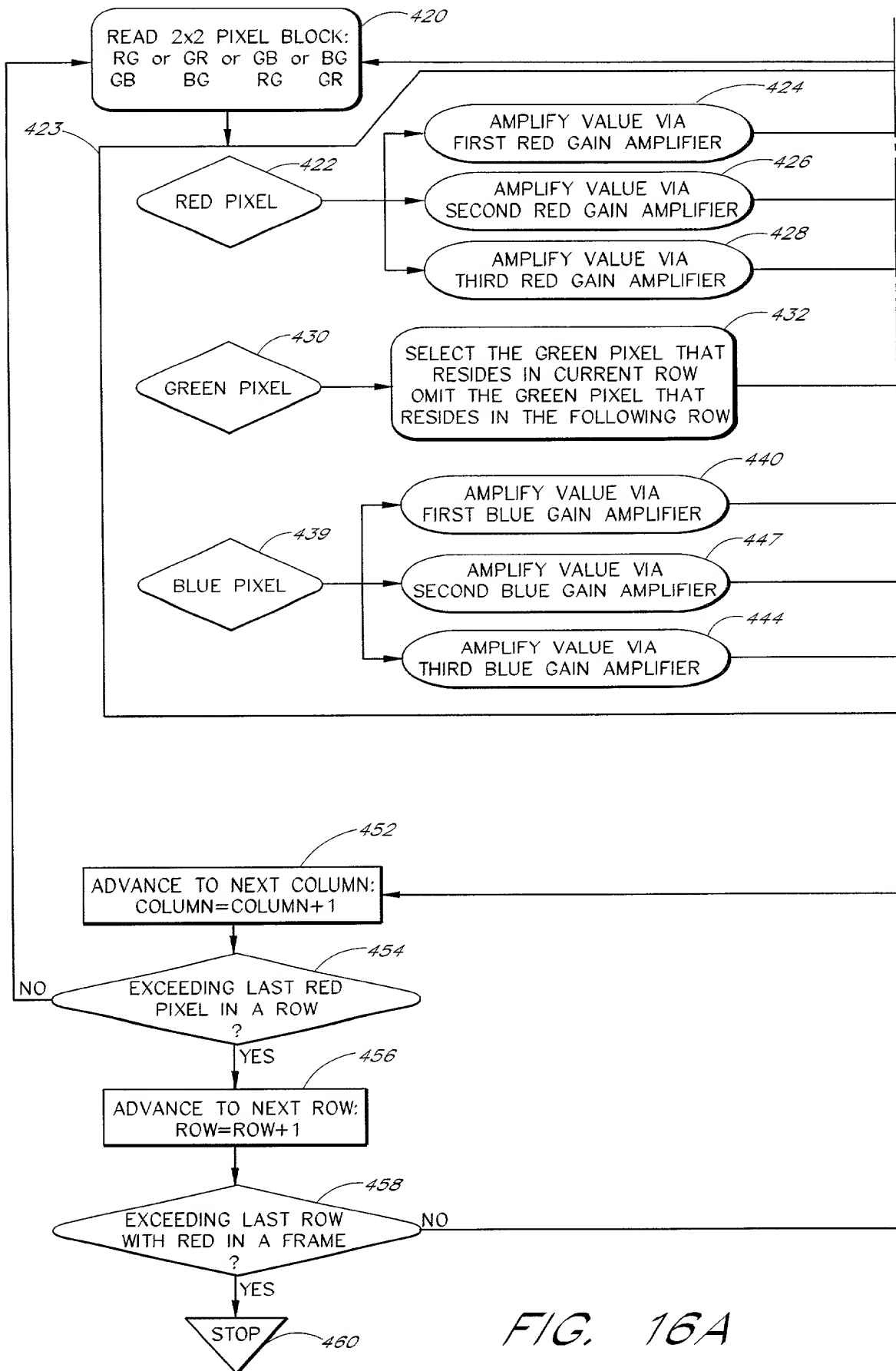


FIG. 16A

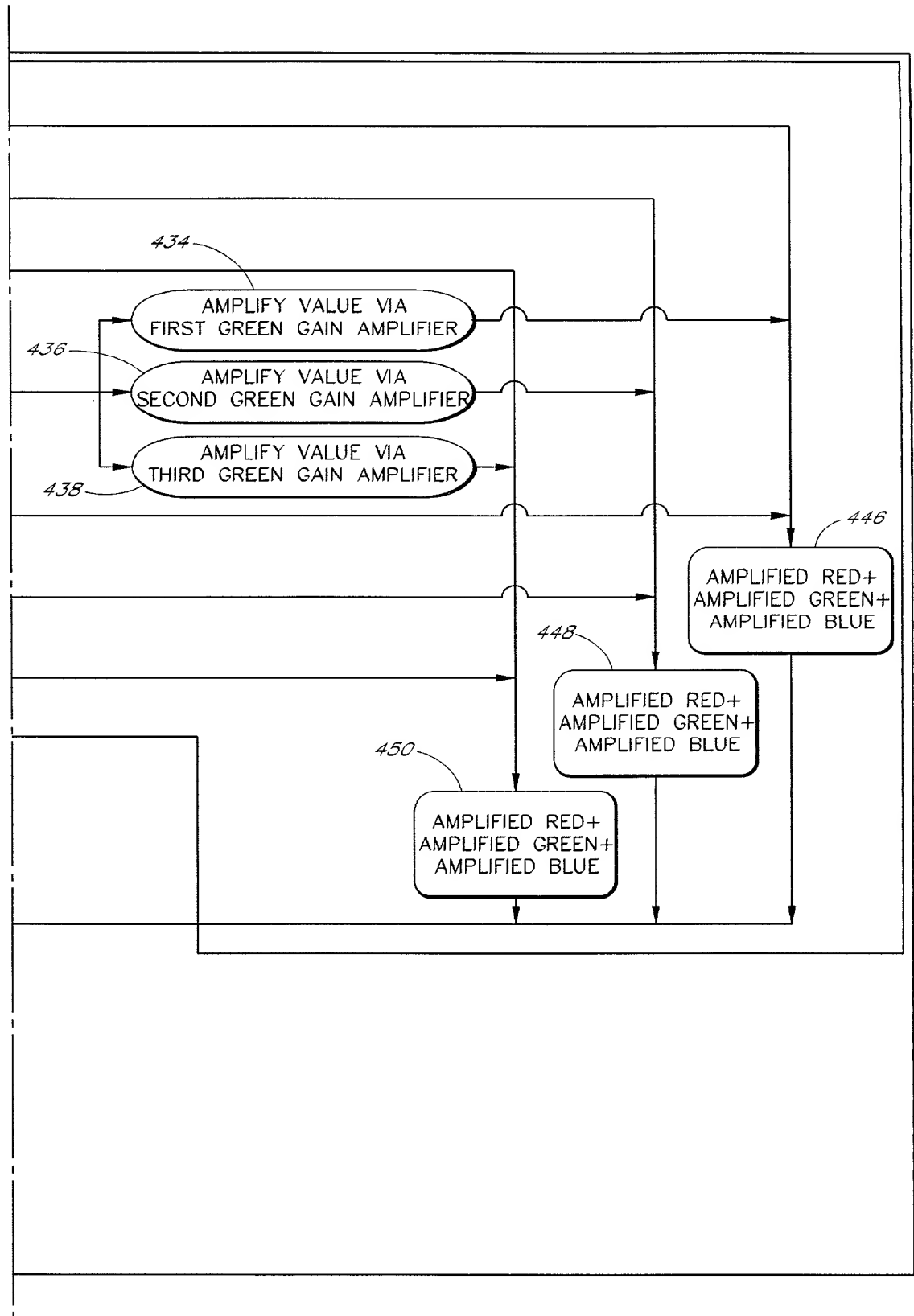


FIG. 16B

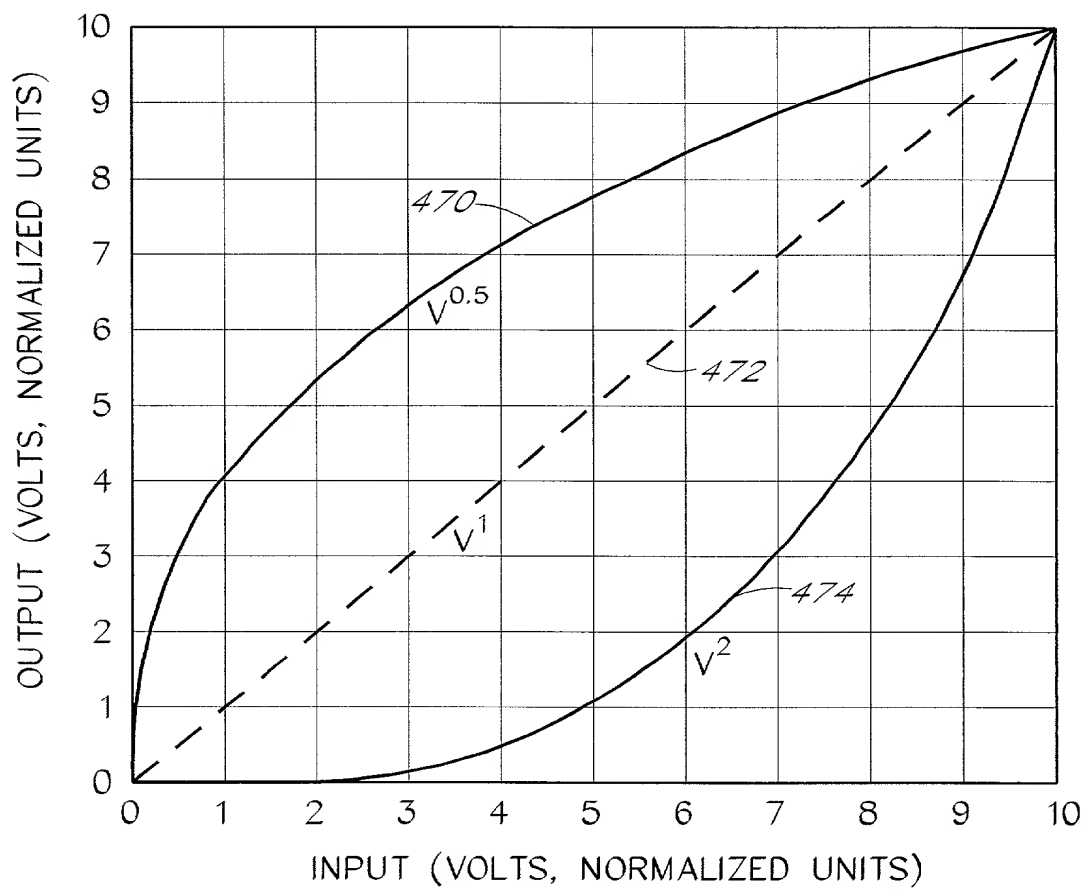


FIG. 17

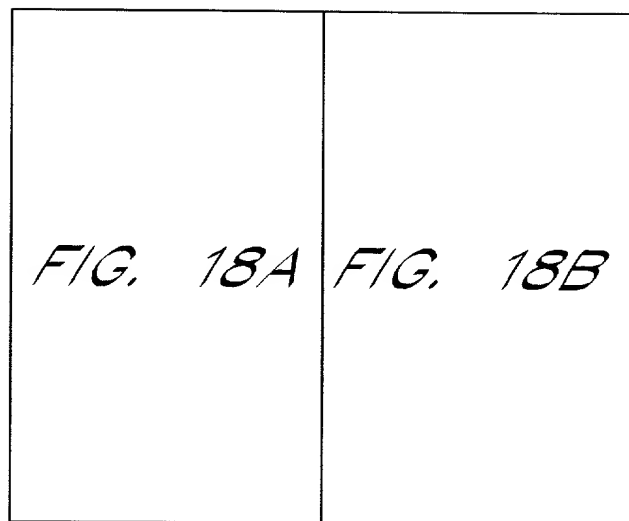


FIG. 18

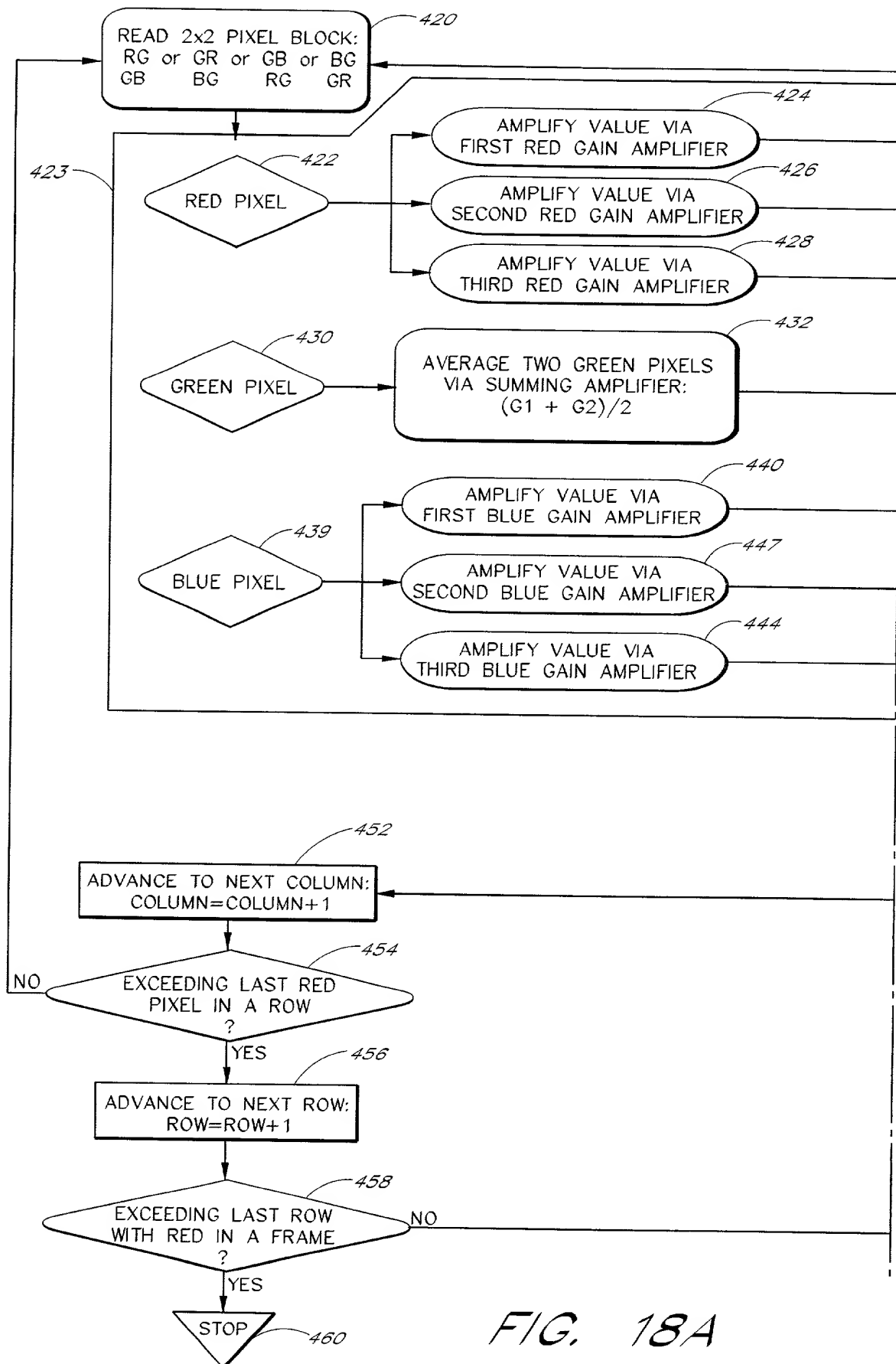


FIG. 18A

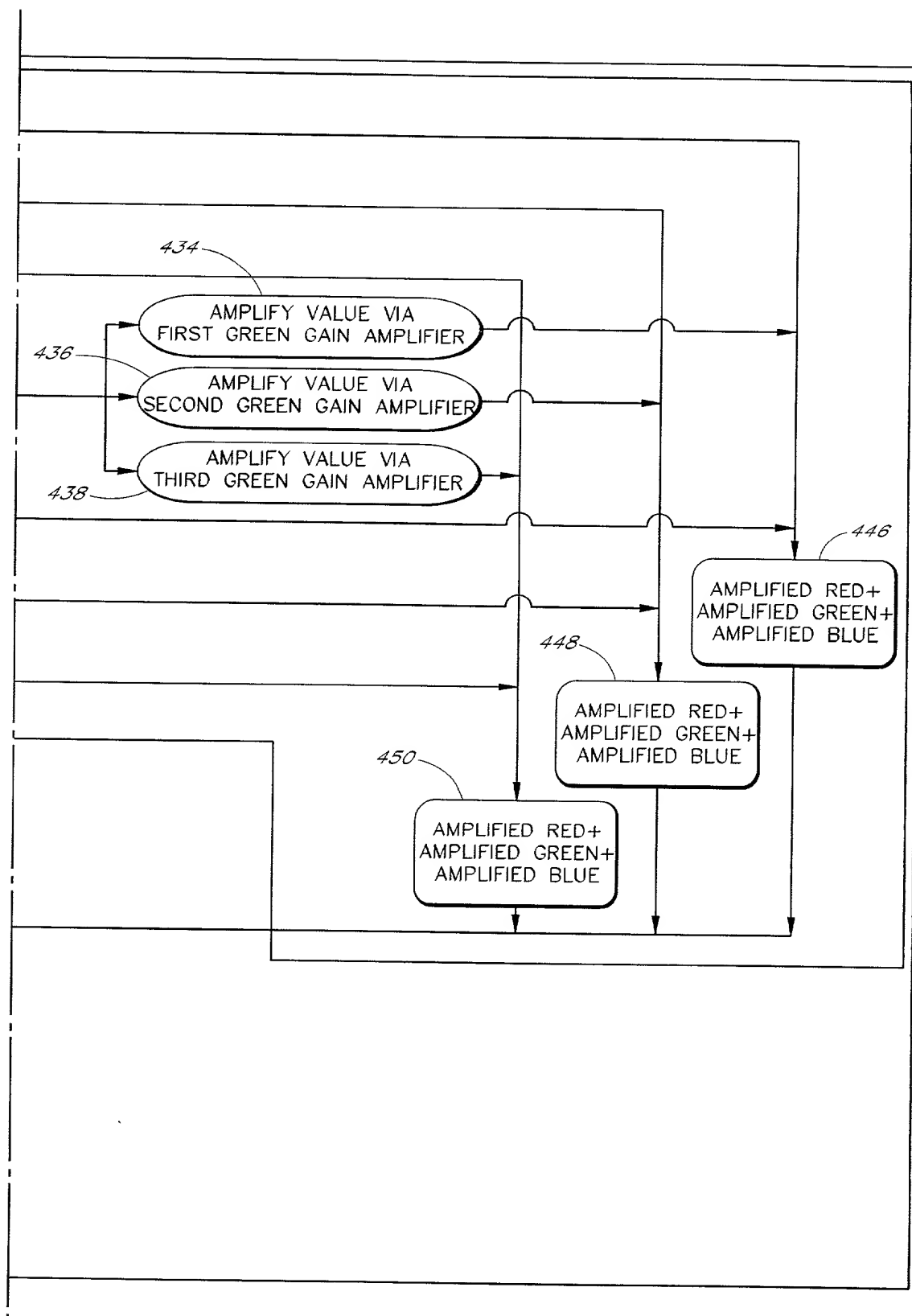


FIG. 18B

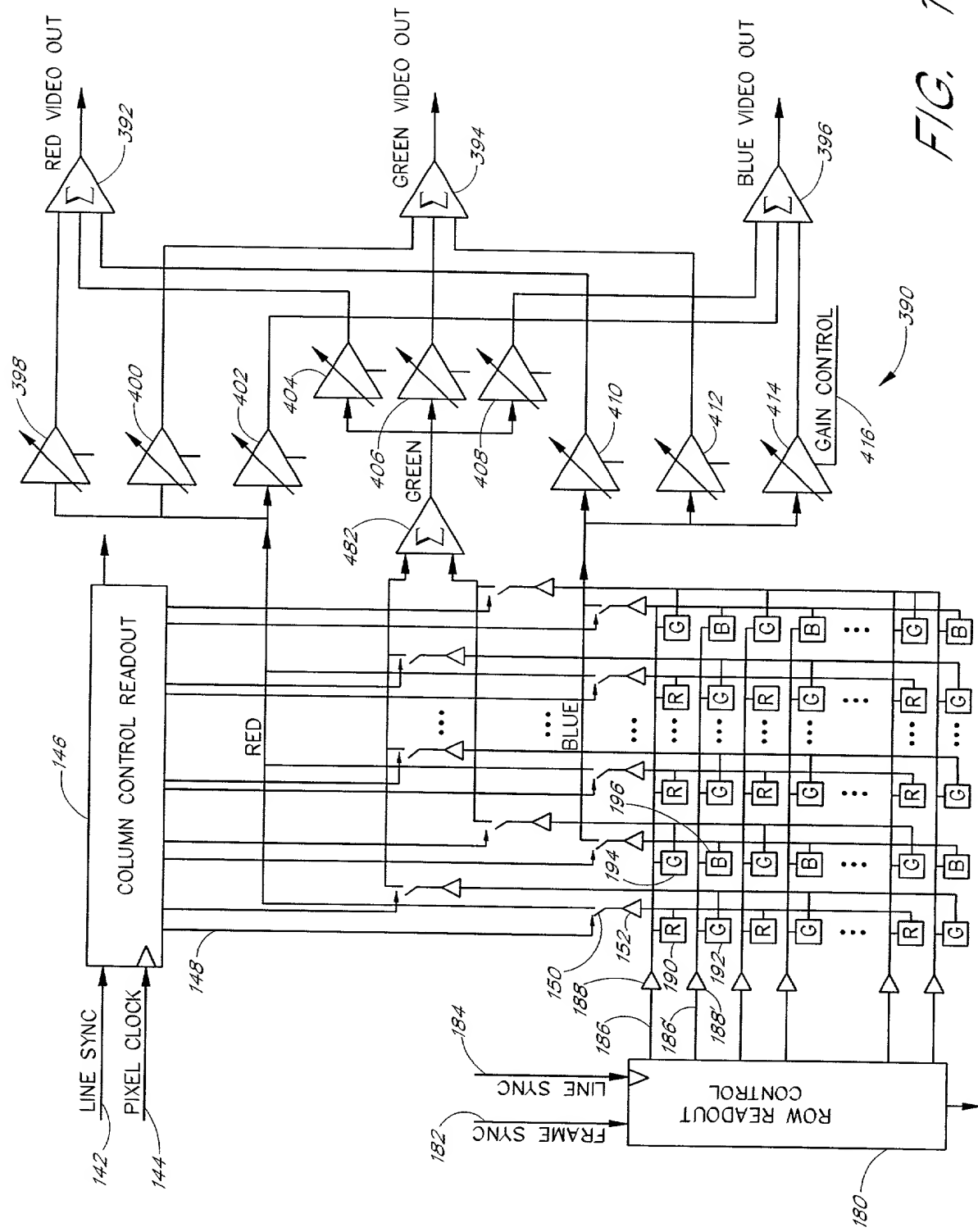


FIG. 19

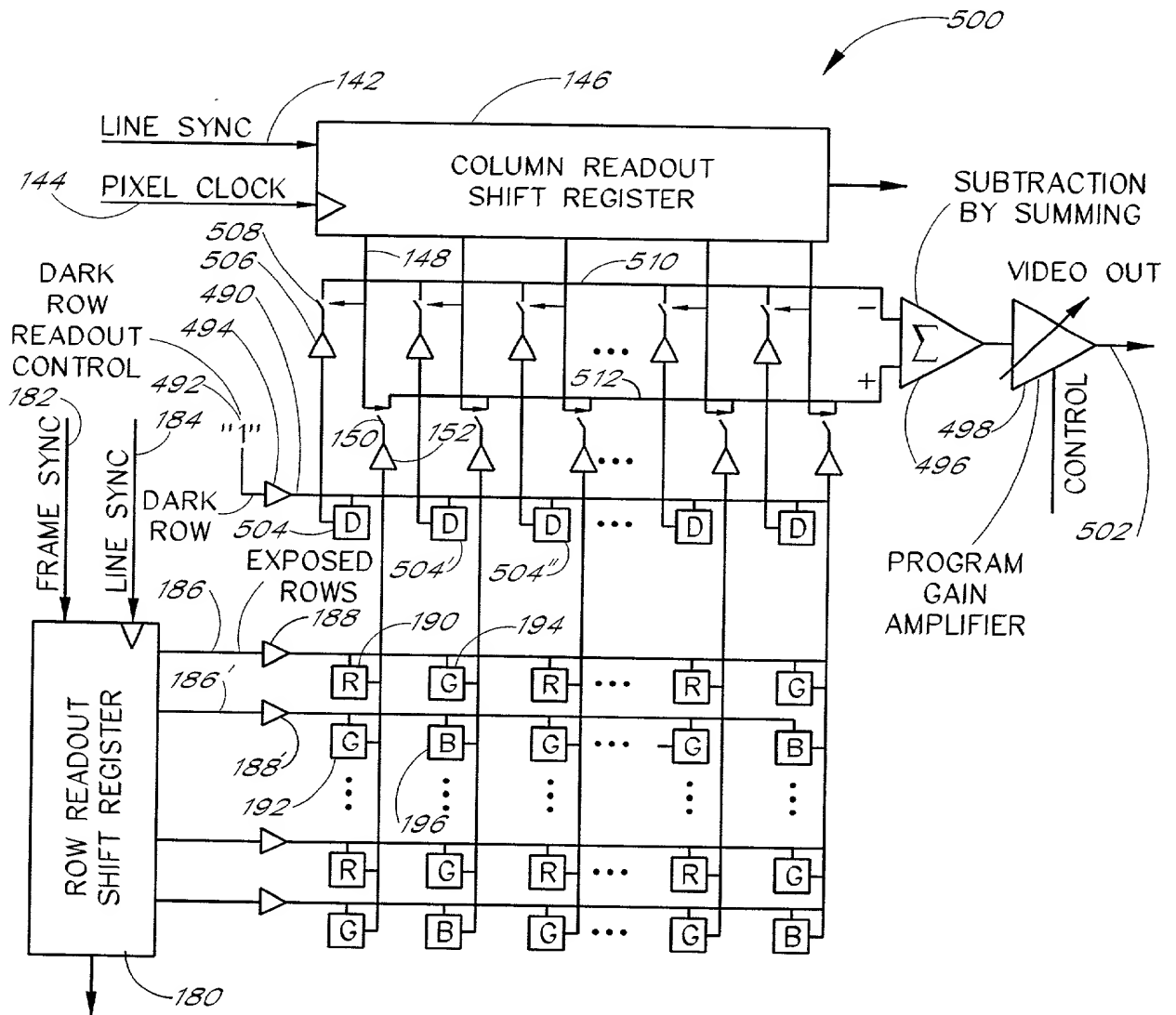


FIG. 20

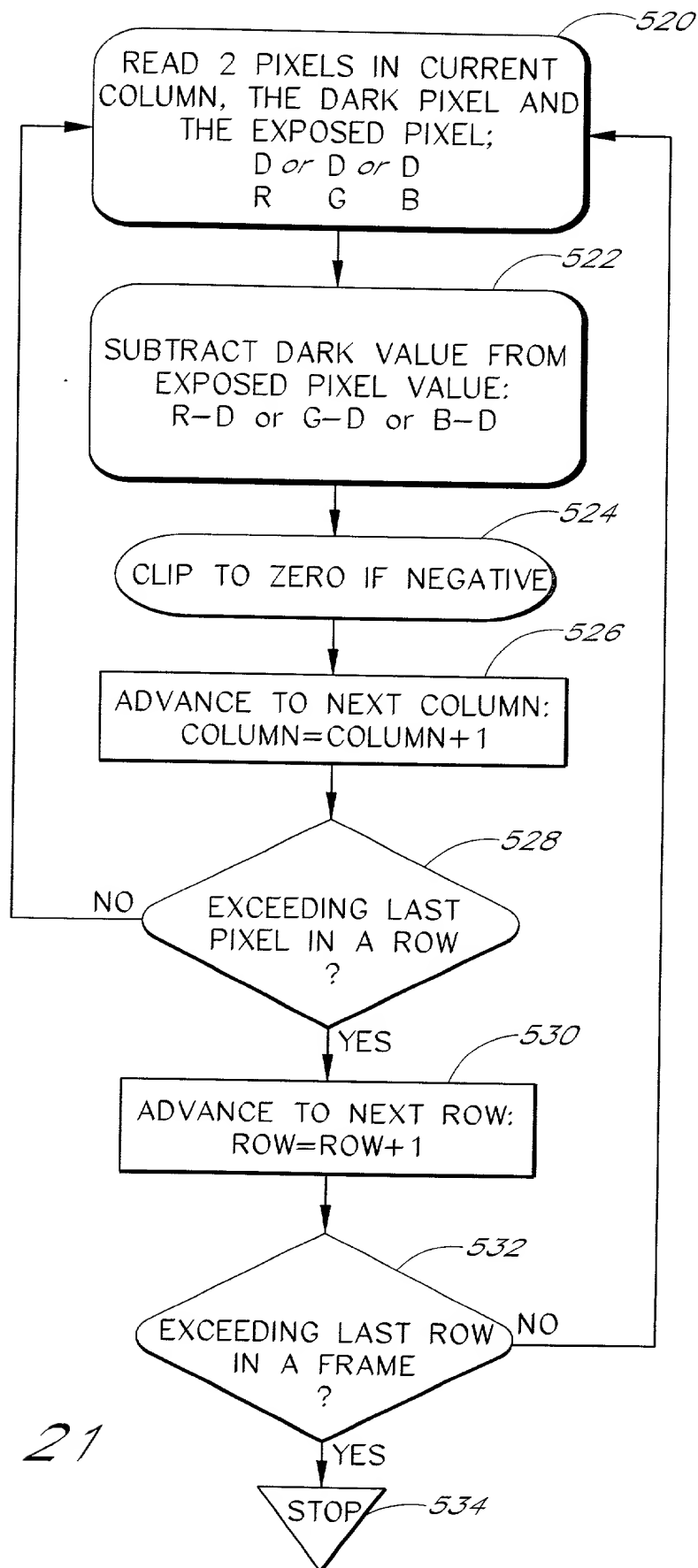


FIG. 21

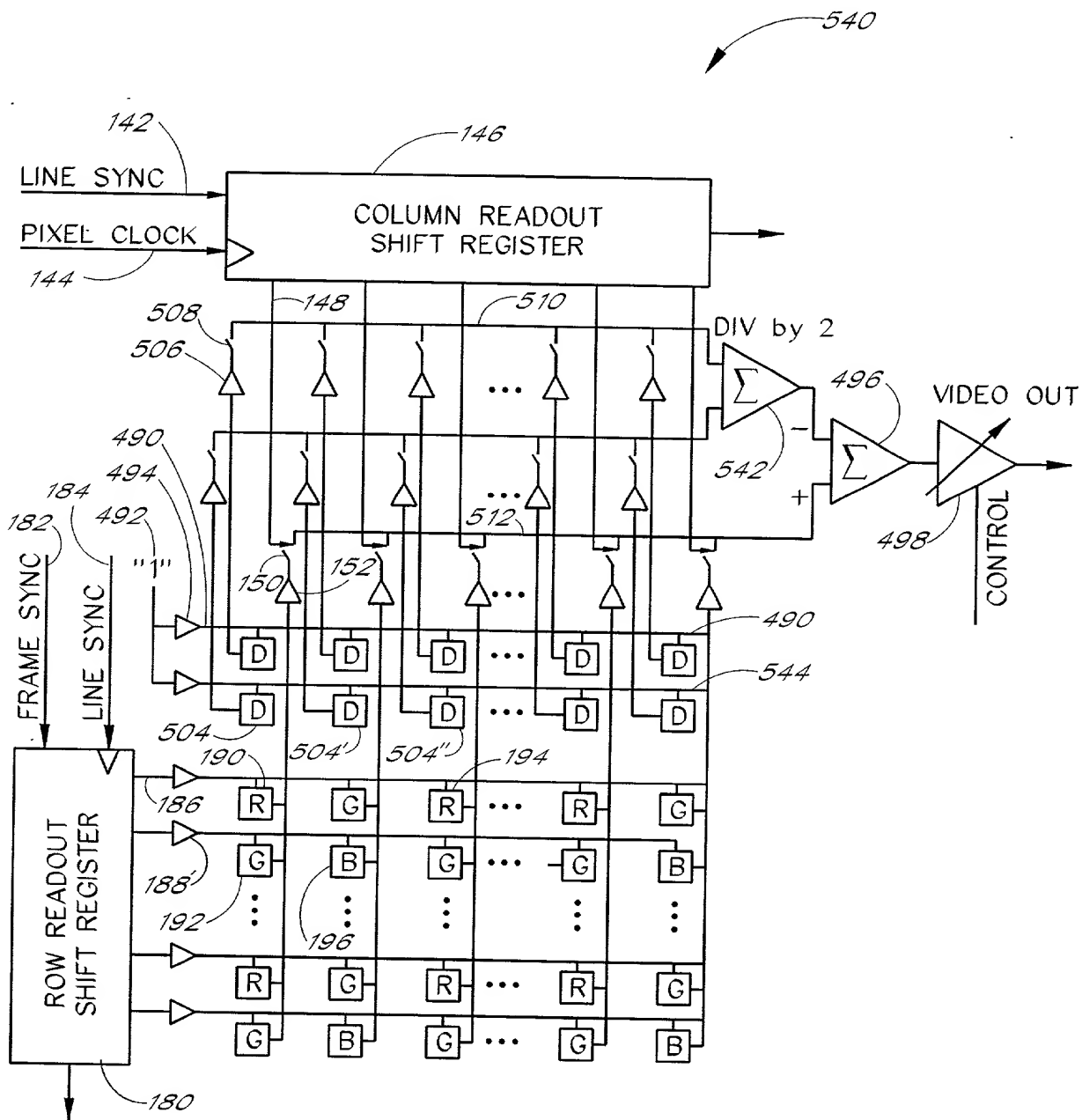


FIG. 22

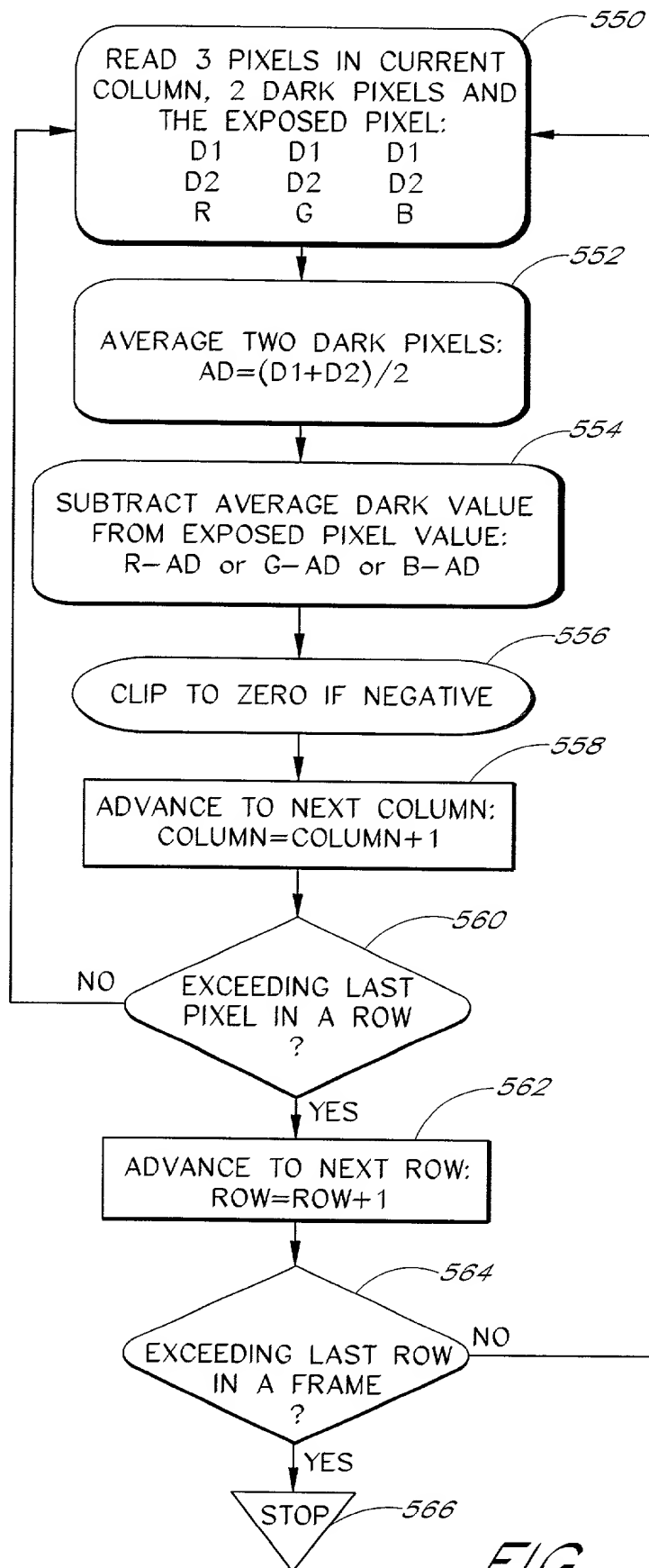


FIG. 23

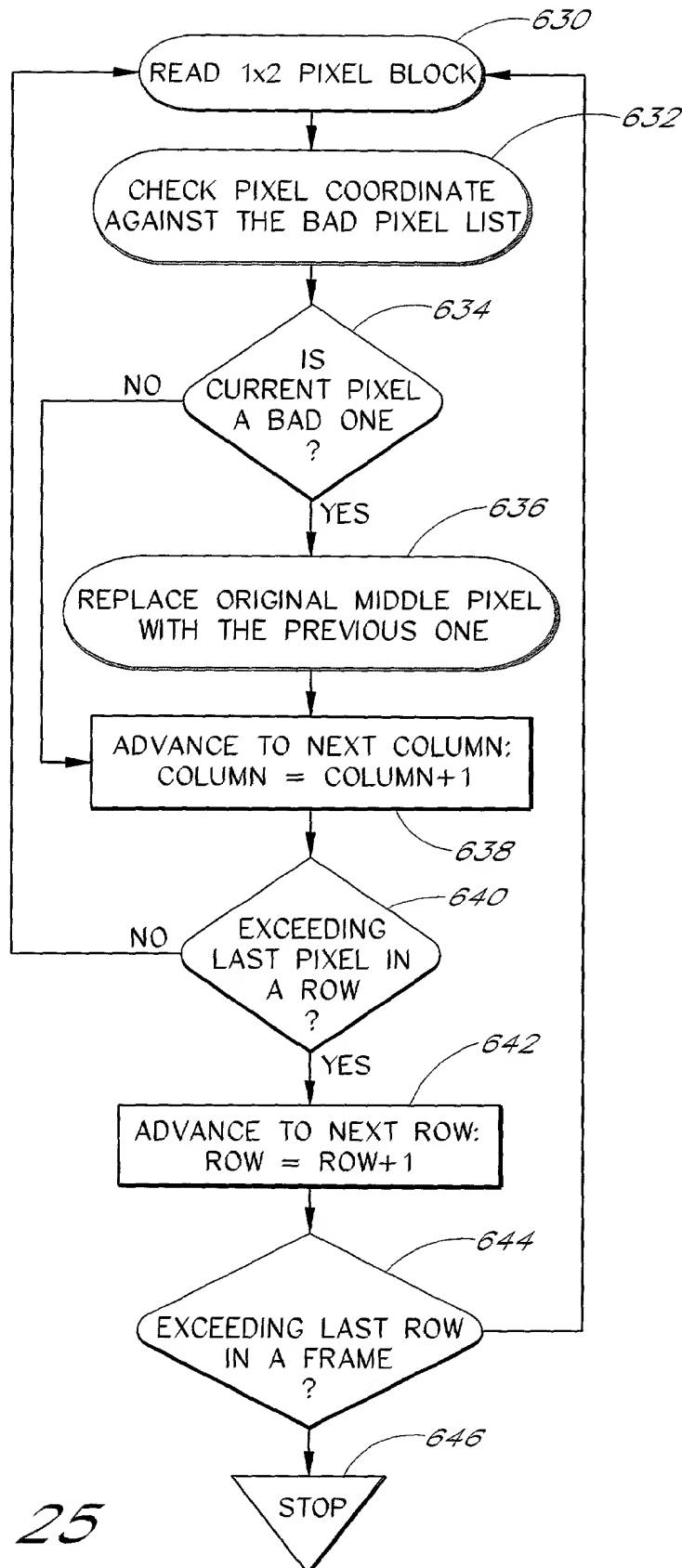


FIG. 25

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD AND APPARATUS FOR COLOR INTERPOLATION; the specification of which is attached hereto;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Codes § 119(e) of any United States provisional application(s) listed below.

Application No.: 60/149,796

Filing Date: August 19, 1999

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole inventor: **Sarit Neter**

Inventor's signature Sarit Neter

Date 2/2/2000

Residence: **15 Highland View, Irvine, CA 92612**

Citizenship: **Israeli**

Post Office Address: **same as above**

Send Correspondence To:

KNOBBE, MARTENS, OLSON & BEAR, LLP

Customer No. 20,995

H:\DOCS\ACC\ACC-1470.DOC:smm
012100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Sarit Neter)
App. No. : Unknown)
Filed : Herewith)
For : METHOD AND APPARATUS FOR)
COLOR INTERPOLATION)
Examiner : Unknown)

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). A true copy of the original Assignment of the above-captioned application from the inventor(s) to the Assignee is attached hereto. This Assignment represents the entire chain of title of this invention from the Inventor to the Assignee.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, 620 Newport Center Drive, Sixteenth Floor, Newport Beach, California 92660, Telephone (949) 760-0404, **Customer No. 20,995**, as its attorneys with full power of substitution and

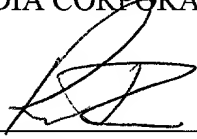
App. No. : Unknown
Filed : Herewith

revocation to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith. This appointment is to be to the exclusion of the inventor and his attorneys in accordance with the provisions of 37 C.F.R. § 3.71.

Please use **Customer No. 20,995** for all communications.

Y MEDIA CORPORATION

Dated: 2-2-00

By: 
Ian Olsen

Title: President & CEO

Address: 23172 Plaza Pointe Drive, Suite 285
Laguna Hills, CA 92653

H:\DOCS\ACC\ACC-1477.DOC
012400